WARSAW UNIVERSITY OF TECHNOLOGY

DISCIPLINE OF SCIENCE - DISCIPLINE OF AUTOMATION, ELECTRONICS, ELECTRICAL ENGINEERING AND SPACE TECHNOLOGIES
FIELD OF SCIENCE - ENGINEERING AND TECHNOLOGY

Ph.D. Thesis

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Control of a Hybrid Transformer to Improve the Power Quality in a Distribution Network

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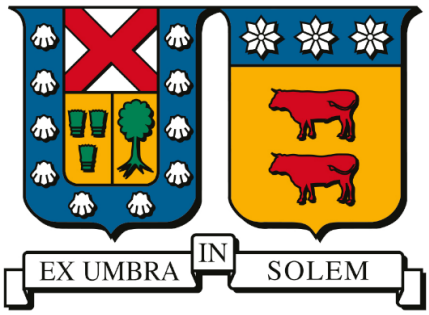
WARSAW 2024

UNIVERSIDAD TÉCNICA FEDERICO SANTA MARÍA
DEPARTMENT OF ELECTRONICS ENGINEERING
VALPARAISO - CHILE



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Doctorate program
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ABSTRACT

Conventional distribution transformers are not capable of dealing with modern and future power systems in which features such as renewable energy systems integration, energy storage, power quality improvement, and bidirectional power flow management are required. To achieve these goals, alternatives to the conventional distribution transformer, such as the Solid-State Transformer (SST), have been proposed. Nonetheless, the SST is far from being a real solution due to reliability and low short-circuit power issues. These problems can be tackled by employing hybrid solutions, such as the Hybrid Distribution Transformer (HDT).

Most HDT configurations comprise a series converter and a parallel converter, where the parallel converter is typically integrated into the main transformer via an auxiliary winding, and the series converter is connected to the secondary side of the transformer. In these configurations, the main transformer is unprotected from the grid voltage and load current disturbances. Even while using the parallel converter to compensate for the nonlinear load currents, and provide sinusoidal currents on the medium voltage side, nonlinear currents circulate through the secondary winding of the transformer. Moreover, the nonlinear currents injected by the parallel converter flow through the auxiliary winding of the main transformer. On the other side, under grid voltage disturbances, the series converter compensates for the voltage disturbances providing a sinusoidal voltage to the load. Nonetheless, polluted and unbalanced voltages are still applied to the transformer terminal. These operating conditions can reduce the lifetime of the main transformer, potentially damaging it.

To address the issues presented in most HDTs, this work proposes an HDT

configuration in which the series converter is connected to the primary side winding, and the parallel converter is connected directly to the secondary side winding. This configuration improves the power quality of the transformer by reducing the THD of the current and the voltage to its terminals while at the same time providing a regulated voltage to the loads. Moreover, retrofitting of the main transformer is potentially allowed.

A discrete-time state feedback controller is designed for the parallel and series converters, in which the main objectives are the improvement of the power quality on the transformer, as well as providing nominal voltage to the loads. The HDT operates under uncertain grid and load conditions. Therefore, in order to preserve the stability of the system, the control algorithm is based on the Linear Quadratic Regulator (LQR). Although the proposed HDT improves the power quality of the system, it requires a Circulating Active Power Flow (CAPF) to work properly. Unless the voltage controller and current controller are degraded or the structure of the HDT is modified, the CAPF is unavoidable. Therefore, part of this work is devoted to its analysis, its impact on the operating conditions, and the efficiency of the HDT.

The main transformer of the HDT can generate inrush currents during and after grid voltage sags or swells. To conclude the thesis and as a proof of concept, the series converter controller is extended and used to regulate the magnetic flux of the main transformer and avoid high-amplitude currents that could jeopardize the grid operation.

***Keywords*—hybrid distribution transformer, efficiency, power quality, discrete-time control, circulating active power flow, voltage and current distortion.**

STRESZCZENIE

Coraz więcej badań dotyczy integracji systemów energii odnawialnej, systemów magazynowania energii oraz wydajnych metod konwersji i poprawy jej jakości. Aby osiągnąć te cele, zaproponowano alternatywy dla konwencjonalnego transformatora dystrybucyjnego transformator półprzewodnikowy (SST), aby poradzić sobie z trudnymi warunkami narzuconymi przez rzeczywiste i nowoczesne systemy elektroenergetyczne. Niemniej jednak, SST jest daleki od bycia rzeczywistym i praktycznym rozwiązaniem ze względu na słabą niezawodność i niską moc zwarciową. Problemy te można rozwiązać poprzez zastosowanie rozwiązań hybrydowych, takich jak hybrydowy transformator dystrybucyjny (HDT).

Większość konfiguracji HDT składa się z przekształtnika szeregowego i przekształtnika równoległego, przy czym przekształtnik równoległy jest zwykle zintegrowany z głównym transformatorem dystrybucyjnym za pośrednictwem uzwojenia pomocniczego, a przekształtnik szeregowy jest podłączony do strony wtórnej tego transformatora. W takich konfiguracjach główny transformator dystrybucyjny nie jest chroniony przed zaburzeniami napięcia sieciowego i prądu obciążenia. Nawet podczas korzystania z przekształtnika równoległego w celu kompensacji nieliniowych prądów obciążenia i zapewnienia sinusoidalnych prądów po stronie średniego napięcia, prądy nieliniowe cyrkulują przez uzwojenie wtórne transformatora. Ponadto prądy nieliniowe wstrzykiwane przez przekształtnik równoległy przepływają przez uzwojenie pomocnicze głównego transformatora dystrybucyjnego. Z drugiej strony, w przypadku zaburzeń napięcia sieciowego, przekształtnik szeregowy kompensuje je, dostarczając do obciążenia napięcie sinusoidalne. Niemniej jednak, zaburzone i asymetryczne napięcia są nadal podawane na

zaciski wejściowe transformatora. Takie warunki pracy mogą skrócić żywotność głównego transformatora, potencjalnie powodując jego uszkodzenie w dalszej perspektywie.

Aby rozwiązać problemy występujące w większości HDT, w niniejszej pracy zaproponowano konfigurację HDT, w której przekształtnik szeregowy jest podłączony do strony pierwotnej, a przekształtnik równoległy jest podłączony bezpośrednio do uzwojenia strony wtórnej transformatora dystrybucyjnego. Taka konfiguracja poprawia jakość zasilania transformatora, zmniejszając THD prądu i napięcia na jego zaciskach, jednocześnie zapewniając regulowane napięcie dla odbiorników. Co więcej, taka modernizacja głównego transformatora dystrybucyjnego jest łatwa do realizacji.

Zaprojektowano dyskretny regulator ze sprzężeniem zwrotnym dla przekształtników równoległego i szeregowego, w których głównym celem jest poprawa jakości energii w transformatorze, a także zapewnienie nominalnego napięcia dla odbiorników. HDT działa w niepewnych warunkach sieci i obciążenia. Dlatego też, w celu zachowania stabilności systemu, algorytm sterowania oparty jest na liniowym regulatorze kwadratowym (LQR). Chociaż proponowany HDT poprawia jakość zasilania systemu, do prawidłowego działania wymaga on cyrkulacyjnego przepływu mocy czynnej (CAPF). O ile w regulacji napięcia i prądu nie zostaną dopuszczone warunki nienominalne lub struktura HDT nie zostanie zmodyfikowana, CAPF jest nieunikniony. Dlatego też część niniejszej pracy poświęcona jest jego analizie, wpływowi na warunki pracy i wydajność HDT.

Podsumowując, główny transformator HDT może generować prądy rozruchowe podczas i po spadkach lub wzrostach napięcia w sieci. W związku z tym jako dowód słuszności koncepcji, sterownie przekształtnika szeregowego zostało rozszerzone i wykorzystane do regulacji strumienia magnetycznego głównego transformatora dystrybucyjnego w celu uniknięcia prądów o wysokiej amplitudzie, które mogłyby zagrozić poprawnemu działaniu sieci elektroenergetycznej.

***Słowa kluczowe*—hybrydowy transformator dystrybucyjny, sprawność, jakość energii, sterowanie dyskretne, cyrkulacyjny przepływ mocy czynnej, zniekształcenia napięcia i prądu.**

RESUMEN

Los transformadores de distribución convencionales no son capaces de tratar con los sistemas de potencia modernos y del futuro, en los que se requieren la integración de sistemas de energía renovables, almacenamiento de energía, mejoramiento de la calidad de la energía, y manejo de flujos de potencia bidireccionales. Para alcanzar estas metas, se han propuesto alternativas al transformador de distribución convencional que permitan manejar las desafiantes condiciones impuestas por los sistemas de potencia actuales y modernos. Una de estas alternativas es el transformador de estado sólido (SST). Sin embargo, el SST aún está lejos de ser aplicable en soluciones reales debido principalmente a problemas relacionados con la confiabilidad y baja potencia de corto circuito. Estos problemas pueden ser abordados empleando soluciones híbridas, tal como el transformador de distribución híbrido (HDT).

La mayoría de las configuraciones de HDTs constan de un convertidor conectado en serie, y otro convertidor conectado en paralelo. El convertidor paralelo es típicamente conectado a un devanado auxiliar, mientras que el convertidor serie es conectado en el secundario del transformador principal. En estas configuraciones, el transformador principal está desprotegido de las perturbaciones del voltaje de la red y de las corrientes de carga. Incluso cuando el convertidor paralelo es utilizado para compensar y mejorar las corrientes que circulan en la red de medio voltaje, las corrientes no lineales de la carga fluyen a través del transformador, como también lo hacen las corrientes de compensación del convertidor paralelo. Por otro lado, al operar bajo perturbaciones de la red de medio voltaje, el convertidor serie compensa el efecto de las perturbaciones en la carga, entregando un voltaje sinusoidal y nominal. Sin embargo, los terminales

del transformador principal están sujetos al voltaje de la red, el cual puede estar distorsionado y desbalanceado. Estas condiciones de operación pueden reducir la vida útil del transformador principal, dañándolo potencialmente.

Para tratar los problemas presentados en la mayoría de HDTs, este trabajo propone un HDT, en el que el convertidor serie se conecta al primario, y el convertidor paralelo se conecta al secundario del transformador principal. Esta configuración permite mejorar la calidad de la energía en el transformador, mejorando el THD de la corriente y voltaje en sus terminales, mientras que al mismo tiempo provee un voltaje regulado a las cargas. Además, la conversión de los transformadores de distribución en operación a HDT es potencialmente posible.

Un controlador de realimentación de variables de estado en tiempo discreto es diseñado para el convertidor paralelo y serie, en el que el principal diseño de control es el mejoramiento de la calidad de la energía en el transformador principal, como también la regulación del voltaje de las cargas. Debido a su naturaleza, el HDT opera bajo condiciones de red y carga inciertas. Por lo tanto, para preservar la estabilidad del sistema, el algoritmo de control es diseñado empleado un controlador cuadrático lineal (LQR). Aunque el HDT mejora la calidad de energía del sistema, requiere un flujo de potencia activa circulante (CAPF) para operar correctamente. A menos que el controlador de voltaje y corrientes sean degradados, o que la estructura del HDT sea modificada, el CAPF es inevitable. Por lo tanto, parte de este trabajo es enfocada a analizar el impacto del CAPF en las condiciones de operación y eficiencia del HDT.

El transformador principal del HDT puede generar corrientes inrush mientras y luego de haber sido expuesto a caídas y sobre tensiones. Para concluir la tesis y como prueba de concepto, el controlador del convertidor series es extendido y utilizado para regular el flujo magnético del transformador, y de esta forma evitar corrientes de alta amplitud que puedan afectar la correcta operación del sistema.

***Palabras clave*—Transformador de distribución híbrido, eficiencia, calidad de la energía, control en tiempo discreto, flujo de potencia activa circulante, distorsión de voltage y corriente.**

ACKNOWLEDGMENTS

First of all, I would like to thank my parents Patricia and Carlos, and my brother Marcel. I feel your support and love constantly. I also would like to thank Anna. Without your support, love, and patience, it would not have been possible to conclude this work.

I would like to thank Professor Marcelo Pérez for giving me his invaluable guidance and support during the development of this thesis. Also, I would like to thank Professor Mariusz Malinowski, who received me in Poland, supported me, and inspired me during the Ph.D. I appreciate having the opportunity to work with both of you.

Finally, I want to thank Professor Marek Jasiński and the research group of GE007B: Tomasz Święchowicz, Sebastian Styński, Tomasz Gajowik, Adam Milczarek, Radek Kot, Cezary Soból, Luis Martinez, Kamil Możdżyński, and Serafin Bachman. Thanks for all the help in the laboratory and for making the time abroad much easier.

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ACRONYMS

ADN	Active Distribution Network
AW	Auxiliary Winding
BESS	Battery Energy Storage System
CAPF	Circulating Active Power Flow
CT	Coupling Transformer
DC	Direct Current
FPGA	Field Programmable Gate Array
GNC	Generalized Nyquist Criterion
HDT	Hybrid Distribution Transformer
HFT	High-Frequency Transformer
LFT	Low-Frequency Transformer
LQR	Linear Quadratic Regulator
MIHDT	Magnetic Integrated Hybrid Distribution Transformer
OPF	Oscillatory Power Flow
PF	Power Factor
PQ	Power Quality
PV	Photovoltaic
PWM	Pulse Width Modulation
STATCOM	Static Compensator
SST	Solid-State Transformer
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Compensator
ZOH	Zero Order Hold

Chapter 1

INTRODUCTION

Remark: This chapter is partly based on the following publication of the author:

[1] A. Carreno, M. A. Perez, C. R. Baier, A. Huang, S. Rajendran, M. Malinowski, "Configurations, Power Topologies and Applications of Hybrid Distribution Transformers", *Energies*, 2021.

Nowadays, there is an increasing interest and high research efforts in achieving a low-carbon and sustainable society, for which the penetration of clean energies such as Photovoltaic (PV) systems, integration of Battery Energy Storage Systems (BESSs), and efficient energy conversion are demanded. In this scenario, systems capable of processing bidirectional power flows, and providing precise voltage and current quality profiles are required. Therefore, the exclusive use of conventional Low-Frequency Transformers (LFT) as an interface between the Low Voltage (LV) grid and Medium Voltage (MV) grid is not sufficient to cope with the demands of the new power systems.

1.1 The conventional and modern distribution grid

Distribution transformers are one of the pillars of the actual distribution grid. They are the interface between the MV and LV grid, stepping down the voltages to a safe and usable range for the end-users. They are characterized by being a highly robust and low-cost solution, being available in different winding configurations and power ratings according to the grid requirement and mounting type [1]. Transformers have an average lifetime above 35 years operating under rated conditions [2].

Power quality (PQ) is a term employed when referring to the power system voltage and current waveform quality at different points of the grid [3]. Low PQ phenomenons can be generated by the users, for example when consuming nonsinusoidal and unbalanced currents. Weak grids can be a source of PQ as well, providing unbalanced and variable frequency voltages. IEEE Std 1159-2019 and IEEE Std 519-2014 give guides on PQ measurements and recommended practices to comply with and guarantee a good quality service [4,5]. Some effects of low PQ are high voltage peaks that can damage equipment, heating, losses, acoustic noise, and lifetime reduction in equipment. For utilities, low PQ is translated into additional losses on transmission lines and generators or the failure of power systems elements that can jeopardize the correct grid operation [6]. The abnormal grid operation can cause considerable economic losses to the operator and end-user. Therefore, PQ problems must not be neglected [7].

Low PQ is more pronounced in distribution systems, due to the high number of variable, nonlinear and unpredictable loads connected to them. As low-voltage distribution grids are supplied by distribution transformers, these can be highly affected by the low PQ presented in these systems. When operating under these conditions, the transformer suffers higher core losses, which increase its hotspot temperature. This is a critical variable, as it is related to the winding isolation degradation and, therefore, decreasing the transformer lifetime [8].

Distribution transformers can be subject to different PQ problems in distribution grids when supplying nonlinear currents and nonlinear voltages [9, 10]. Industrial applications, such as elevators, rolling mills, arc furnaces, among others, consume high amounts of current in short periods, worsening distribution grid operation. PQ issues, such as flickering, can be generated due to the operation of industrial machinery [11]. Additionally, new kinds of loads establish new operating conditions for distribution transformers and the grid, for which they were not designed. For example, high penetration of wind and PV systems connected to the grid through power converters adds a degree of uncertainty to the grid operation due to the high variability of these

resources and also due to the harmonics injected by the power converters [12]. The distributed characteristic of these systems makes it possible that the voltage profile on the distribution grid can increase close to the connection points under high penetration periods [13]. This scenario can represent a problem for grid control systems, such as transformer tap changers, making them switch when it is not required [14]. On the other side, the widespread of electric vehicles can overload the grid. Charging algorithms for electric vehicles tend to delay the vehicle charging process to the night, due to economic incentives [15]. This scenario can overload the distribution transformers, reducing their lifetimes [16]. Several methods are proposed to reduce the impact on distribution transformers—for example, utilizing the power converter of distributed renewable energy resources for volt-var control, smart control system, intelligent and coordinated charging algorithms and including the distribution transformer hotspot model into the power converter control systems, the use of BESS in order to operate in periods of high energy demand, among others [16–18].

The regulating capabilities provided by a distribution transformer are limited. To deal with slow dynamic voltage variations, they are provided with on-load taps commutating systems, which allow for modifying the winding ratio without disconnecting the load. Nonetheless, these systems operate in a discrete manner and with dynamics in the order of seconds. Additionally, they are the main transformer failure cause, which jeopardizes the distribution grid, adding additional maintenance costs [19]. The use of electronic-assisted taps commutating systems is available, allowing for a decrease of the commutation times and losses. Nevertheless, they suffer additional conduction losses and operate in discrete voltage steps as well [20]. Distribution transformers do not have mechanisms to mitigate load current harmonics, being necessary to design them to operate under these conditions. These transformers are known as k-rated transformers [21].

Solid-State Transformers (SSTs), shown in Fig. 1.1(a), are an attractive solution to cope with PQ problems. In this scenario, the conventional distribution transformer is fully replaced by a power electronics converter. Normally, SSTs consist of several conversion stages, which can be seen in Fig. 1.1(b). They are based on power electronics combined with High-Frequency Transformers (HFTs), allowing for fast and precise voltage and current control [22]. Some characteristics and advantages of SSTs are given below [23].

- High-quality voltage supply: Grid voltage disturbances, such as voltage unbalances and harmonics can be isolated, providing a sinusoidal voltage to the low-voltage side.

- High-quality grid currents: For example, SSTs can provide current harmonic mitigation, Power Factor (PF) correction and load balancing, and therefore improve

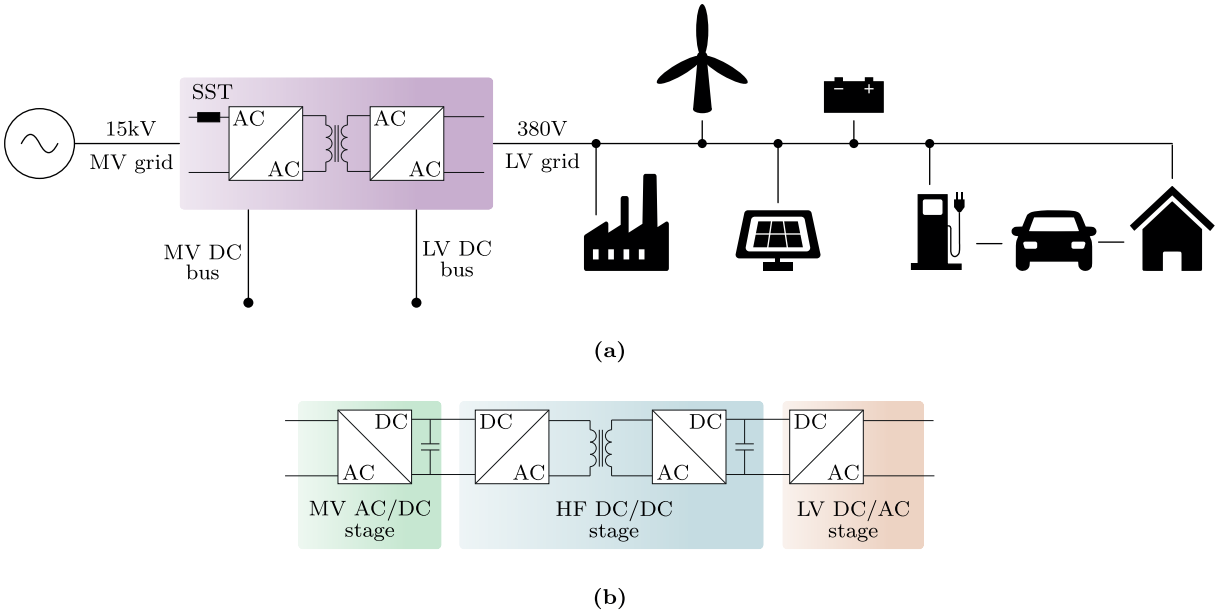


Fig. 1.1. Solid-State Transformer concept. **(a)**. Generalized SST in a MV to LV distribution grid. **(b)** Typical conversion stages of an SST.

the current quality of the MV grid.

- DC port availability: Due to the conversion stages and depending on the SST topology, MV and LV DC buses are available.
- SSTs allow the integration of renewable energy systems and energy storage.
- Modularity and scalability
- Smart load management and advanced monitoring

Nonetheless, the efficiency of these systems is lower compared to other existing solutions, due to the necessity of operating with a high number of submodules and power conversion stages, and the processing of the complete power flow. Compared to a distribution transformer, the complexity of an SST, the additional power electronics, and the cost prevent the SST from being applied in the actual power systems [24]. However, the main reason relies on the reliability issues suffered by the SST. Distribution grids can be subject to different kinds of faults, in which short circuits can be highlighted. These high-amplitude currents can not be supplied by the STT without considering countermeasures, such as overrated design, incorporating rotating machines, and internal reconfiguration [25]. Therefore, hybrid solutions that lie between the conventional distribution transformer and the SSTs can be a promising solution.

1.2 The Hybrid Distribution Transformer (HDT)

The concept of Hybrid distribution transformers (HDTs) is shown in Fig. 1.2(a), and they combine a distribution transformer with one or more power electronics conversion stages, which are designed to operate at a fraction of the nominal power of the distribution transformer. HDTs have attracted the attention of the industry, where ABB has filed several patents relating to their control, configurations and applications [26–29].

Nowadays, the available configurations, topologies, and control objectives are diverse. As can be seen, the HDT is the interface between the MV and LV grid, where the HDT is any nonspecific combination of power electronics modules connected with the distribution transformer [30]. Compared to the SST, the power converter stage corresponds to a partial power converter, and therefore the control capabilities are limited to the power converter rating. Typically the power converters are designed to operate at between 10% and 20% of the transformer nominal power [31]. Additionally, for the same reason, the efficiency of the power converter stages has a low impact on the overall conversion efficiency. The use of protection systems, such as bypass switches, varistors, and DC-Link clamping circuits, increases the power converter losses and volume. Nonetheless, due to the partial power converter, the protection systems have an insignificant impact on the overall efficiency and volume [32, 33]. There is no restriction on the power converter location, with works reporting several different connection possibilities, i.e., MV and LV side connections, each with its own advantages and disadvantages. Therefore, the HDT configuration and power converter location will determine the power converter topology, semiconductors rating, and the compensation that the HTD can provide [34].

Fig. 1.2(b) shows a highly researched HDT, in which the power converters are connected to an Auxiliary Winding (AW), and also in series with the LV grid [32]. This HDT employs an LFT with open winding, as shown in Fig. 1.2(c).

One of the main concerns with the applicability of new technologies in the grid is power system reliability. LFT can operate for several seconds under grid failures, such as short circuits. In contrast, power converters have a very limited short-circuit current supply capacity. In this regard, some HDT configurations can operate under faults, as the HDT configuration allows for the power converter to be disconnected during the fault, letting the LFT supply the short circuit currents, preserving the grid reliability [32].

Each HDT configuration and topology must be considered in the design of the HDT to provide a reliable operation; nonetheless, not enough research has been carried out in this area. In general, for HDTs with series-connected converters, it is considered a bypass switch that short circuits the power converter in the case of faults [31, 35]. For

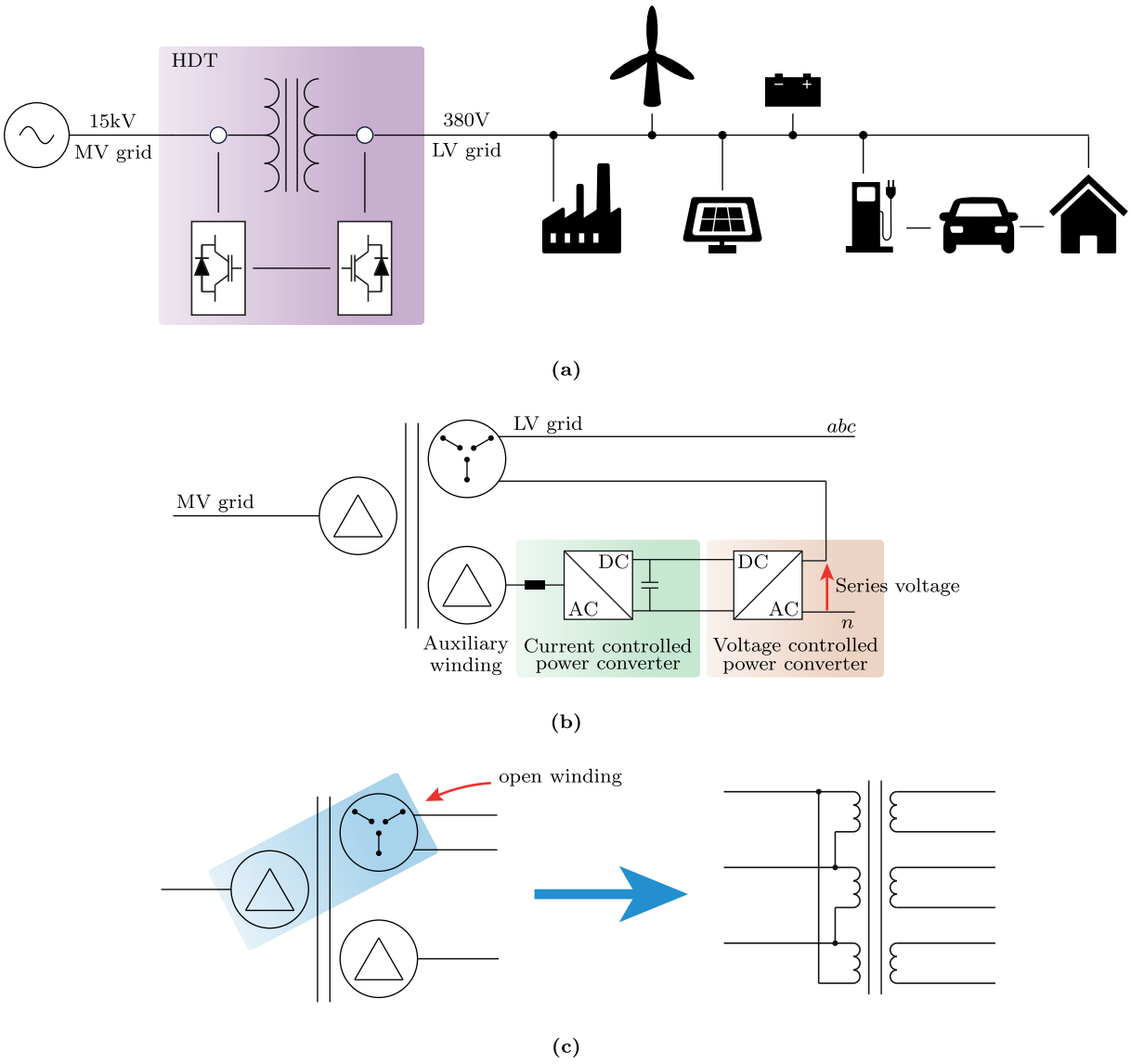


Fig. 1.2. Hybrid Distribution Transformer. **(a)** Concept. **(b)** Example HDT [32]. **(c)** Open winding configuration.

the configuration of Fig. 1.3, a comprehensive protection system design has been realized [32,33]. In the case of short circuits on the low-voltage grid, high currents are delivered by the transformer and the power converter. Therefore, in this situation, the power converter must be bypassed rapidly, allowing the transformer to deliver the short circuit currents. A bidirectional switch composed of antiparallel high current thyristors, S_2, is utilized, which provides a low-impedance path in less than $100\mu s$. Then, after the system is correctly bypassed, an additional mechanical switch, S_{m2} is activated to reduce the losses. At the same time, the mechanical switch for the parallel converter, S_{w1}, is utilized to connect the parallel converter during startup and disconnect it during failures. Additionally, the

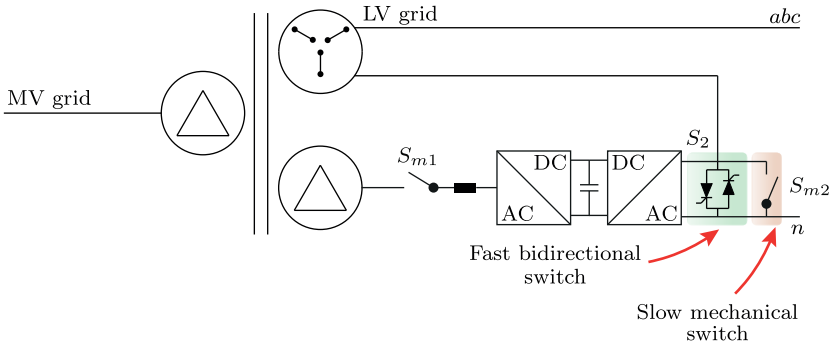


Fig. 1.3. Hybrid transformer with bypass switch.

reliable design of the HDT considers diverse scenarios, such as lightning surges and MV surges, for which it is necessary to find a compromise between the AW ratio, power converter losses, semiconductor breakdown voltage, and filter size, among others.

A reliable HDT must be able to detect a dangerous operating condition and depending on the configuration, bypass and/or disconnect the power converter from the grid and transformer [35]. When done correctly, the HDT behaves as a conventional LFT, ensuring high reliability. Alternatively, reliability can be assessed according to the power converter topology and its under-fault operation capability. For example, for two-level converters, redundant legs can be included which can be switched on in the case of faults. Additional fault isolation circuits are mandatory to isolate the damaged leg as fast as possible [36]. On the other hand, for configurations connected to the MV side, the use of MV multilevel converters adds a level of reliability compared to, for example, two-level topologies. When a submodule of a cascaded multilevel converter fails, the system can be reconfigured to continue with its normal operation, without requiring to disconnect the power converter [37]. Nonetheless, the complexity and cost of the implementation scale up.

1.3 HDT configurations

In this work, the HDT configurations are classified according to the energy source of the power converter unit, as follows:

- Floating capacitor.
- MV or LV side winding of the main LFT.
- AW of the LFT.

Simultaneously, each one can be classified according to the method utilized by the power converter to inject its energy into the grid, which is directly related to the kind of compensation it can provide. The injection methods can be classified as:

- Series injection.
- Series injection through Coupling Transformers (CTs).
- Parallel injection.
- Magnetic compensation.

The HDT configurations, classified with respect to the energy source of the power converter and the injection method are summarized in Fig. 1.4.

In this section, HDT configurations are categorized regardless of the phase numbers of the grid, assuming that the power converter is fully controllable. Additionally, it is only in self-supported HDTs that the conversion method is shown, whereas in the remaining configurations, the power converters are generalized as AC/AC power converters. Although the operation region and injection capability are strictly tightened to the power converter topology, it is assumed that the power converters operate in a decoupled manner, and both terminals operate in the four-quadrant region [38].

1.3.1 Self-supported HDTs

Self-supported HDTs, or HDTs where the energy is obtained from DC capacitors, are presented in Fig. 1.4(a)–(d). Regardless of the power converter connection method, the power converter can only provide reactive power compensation when utilizing DC capacitors as the energy source. An additional control method based on active power is required to charge and regulate the capacitor voltage to its rated value. Active power compensation can be provided when integrating DC sources into the DC-Link.

The configuration of Fig. 1.4(a) is utilized to provide voltage regulation to the distribution grid [30]. No isolation is required when the power converter is connected between the neutral point and the LFT winding. Moreover, if the neutral point is inaccessible, connecting the power converter to the distribution line without CTs is possible by utilizing single-phase power converter topologies [39]. Alternatively, the integration to the distribution grid can be realized utilizing CTs, as configuration Fig. 1.4(b) shows, allowing for the use of three-phase power converter topologies instead of single-phase configurations, reducing the converter elements. Integrating a DC source into the DC-Link, such as a battery bank, allows voltage control utilizing active power,

Fig. 1.4. One-line representation of the HDT configurations. **(a)** Power converter connected in series without a coupling transformer (CT). **(b)** Power converter connected in series with CT. **(c)** Power converter connected in a parallel configuration. **(d)** Power converter coupled to the core of the LFT. **(e)** Power converter connected to AWs and in series without CT. **(f)** Power converter connected to AWs and in series with CT. **(g)** Power converter connected to two AWs. **(h)** Power converter connected to the LV side and in series without CT. **(i)** Power converter connected to the LV side and in series with CT. **(j)** Power converter connected to the MV and LV sides of the LFT in a parallel configuration.

extending the converter regulation capabilities [40]. Additionally, thanks to the CTs, the power converter can be connected to the MV grid [41].

The configuration of Fig. 1.4(c) provides shunt compensation by connecting the power converter to the LV side [30]. This configuration can be integrated into the LV distribution grid with or without CTs [42]. It is possible to utilize the same configuration connected to the MV side. Nonetheless, unless multilevel power converter topologies are employed, CTs are required to connect the converter output due to the higher voltage levels [43]. Alternatively, MV semiconductors have been researched to achieve a direct connection to the MV grid [44, 45]. Another alternative to cope with the connection to MV is to utilize the LFT taps to reduce the AC voltage connection level and the minimum required DC-Link voltage. This solution has been proposed as a Static Synchronous Compensator (STATCOM) integrated into the LFT with and without passive filter branches [46]. Nonetheless, the current distribution of the MV winding is not equal, causing overcurrents and damaging the windings. Therefore, the reactive power compensation must be limited according to the load PF in order to avoid failures [47]. The same idea has been proposed and applied to the LV side taps, to additionally provide active filtering [48].

It is possible to connect the power converter to an AW of the LFT to provide magnetic compensation, as Fig. 1.4(d) shows. In this case, the LV winding and AW share the same core path and, therefore, the same magnetic flux, equivalent to a power converter connected in an electrical parallel configuration [30]. One application of this configuration provides current filtering in large-power industrial rectifiers and shipboard power systems [49, 50]. The AW can contain tuned filter branches, which can be actively controlled to mitigate characteristics harmonics of nonlinear systems [51].

1.3.2 HDTs connected to auxiliary windings

The HDT configurations presented in Fig. 1.4(e)–(g) correspond to those configurations in which the power converter obtains its energy from an AW of the LFT. The main characteristic of these configurations is that the AW provides magnetic isolation, allowing the synthesis of a single-phase voltage, which can be connected in series to the distribution line. Then, depending on the system phase numbers and power converter characteristics, one of the three configurations should be utilized, as explained below.

In the configuration of Fig. 1.4(e), the power converter can be connected in series to the secondary side of the transformer if:

1. The transformer has an open windings configuration
2. The neutral connection must be realized on the power converter side

Most of the research studies on HDTs have focused on this configuration, and different power converters have been applied to it. Additionally, several patents that utilize this configuration have been filed by ABB [26–29]. HDTs based on unidirectional power converters have been proposed. Nonetheless, their operation region highly depends on the grid and load conditions [52]. On the other hand, solutions based on back-to-back AC/DC power converters extend the regulation capabilities, providing voltage and current control in a broader range [53]. Additionally, it is possible to utilize AC/AC chopper converters. Nonetheless, the regulation capabilities depend on the utilized power converter topology and the grid impedance matching. Moreover, depending on the converter topology, under grid faults, and after bypassing the power converter, the LFT cannot provide rated voltage due to unconventional ratios of the secondary and AWs. These issues are solved by utilizing bipolar AC/AC power converters [35]. Another alternative is to utilize three-phase AW for each output phase in conjunction with DC-Link-based power converters. In this case, independent DC-Links per phase are required, simultaneously allowing for connecting the power converter in series to the distribution line without CTs after the LFT output terminals. The three-phase output voltages are magnetically isolated between them. Moreover, different winding configurations can be utilized to mitigate harmonic currents generated by the power converter switching process [54].

In the configuration of Fig. 1.4(f), the series converter is integrated into the distribution grid through CTs. In conjunction with the CT, the AW isolates the power converter from the grid, which allows for optimization and reduction of the DC-Link voltage independently of the series converter location. There are solutions based on back-to-back AC/DC converters [34], as well as based on AC chopper converters [55, 56]. Connecting the series converter to the MV side can protect the LFT from grid voltage disturbances, providing the required mitigation on the MV grid [57]. A detailed model and compound control scheme has been presented for this configuration. The model accounts for the voltage and current disturbances, aiming to improve the robustness of the system [58]. Additionally, controllable tuned filter branches have been proposed for the shunt converter to mitigate characteristics harmonics. The power converter can actively regulate the filter impedance for harmonics mitigation purposes [59].

An alternative to the previous configurations is the Magnetic Integrated Hybrid Distribution Transformer (MIHDT), shown in Fig. 1.4(g). This configuration fully integrates the power converter into the main LFT. In this case, the power converter takes its energy from an AW, which, after being processed, is injected back into the LFT through an additional AW. The core and winding configuration determine the purpose of the power converter.

One specific configuration of MIHDT has been published as a Power Electronics

Integrated Transformer (PEIT) and Custom Power Active Transformer (CPAT). Two equivalent parallel electrical circuits can be realized using two windings sharing the same magnetic core path, whereas a series electrical circuit is made by a winding attached to a third core leg or a shunt magnetic core path [60]. A single-phase PEIT has been proposed, whereas the three-phase alternative is obtained by connecting three single-phase PEITs [61]. In order to increase the level of integration, a shell-type structure is utilized, sharing the transformer yokes, which finally reduces the transformer footprint [62]. This configuration can be utilized as a power flow controller while providing current and voltage harmonics mitigation [63]. Another MIHDT has been proposed, which is shown in detail in Fig. 1.5 [64]. In this HDT, the main LFT integrates the CTs into the main core, as well as the power converter filter inductors. The latter are not shown in the diagram in order to simplify it. This alternative allows for a reduction of the amount of magnetic material and copper utilized.

1.3.3 HDTs connected to transformer windings

Configurations of Fig. 1.4(h)–(j) show HDTs where the power converters obtain their energy from the MV or LV windings of the LFT. Since the power converter is directly connected to the windings of the LFT, an isolation stage is required to synthesize an isolated series voltage or to maintain the isolation between the MV and LV grid when it is required. As shown in the presented configurations, this task can be done through CTs or internal-isolated power converters.

In the configuration of Fig. 1.4(h), the power converter takes its energy from the LV winding, and after processing it, it is injected in series to the distribution line. The transformerless series connection is possible due to an internal isolation stage based on HFTs. This configuration has been proposed for a single-phase HDT, which, compared to solutions based on CTs and connected to AWs, allows for a reduction in weight and volume while being a retrofit and scalable solution [65–68]. On the other side, the configuration of Fig. 1.4(i) provides current and voltage compensation on the LV side. This configuration requires the use of CTs to allow the injection of a series voltage to the distribution line. This configuration is proposed based on back-to-back DC-Link-based power converters [53], and with three-phase direct AC/AC converters as well [69].

In Fig. 1.4(j), the power converter is connected to the MV and LV side in a parallel configuration utilizing power converters isolated by HFTs. For example, this configuration is utilized for the integration of renewable energy systems or when it is desired to increase the distribution transformer capacity without replacing it. In principle, this configuration does not allow proving series voltage regulation directly; nonetheless, it can be controlled

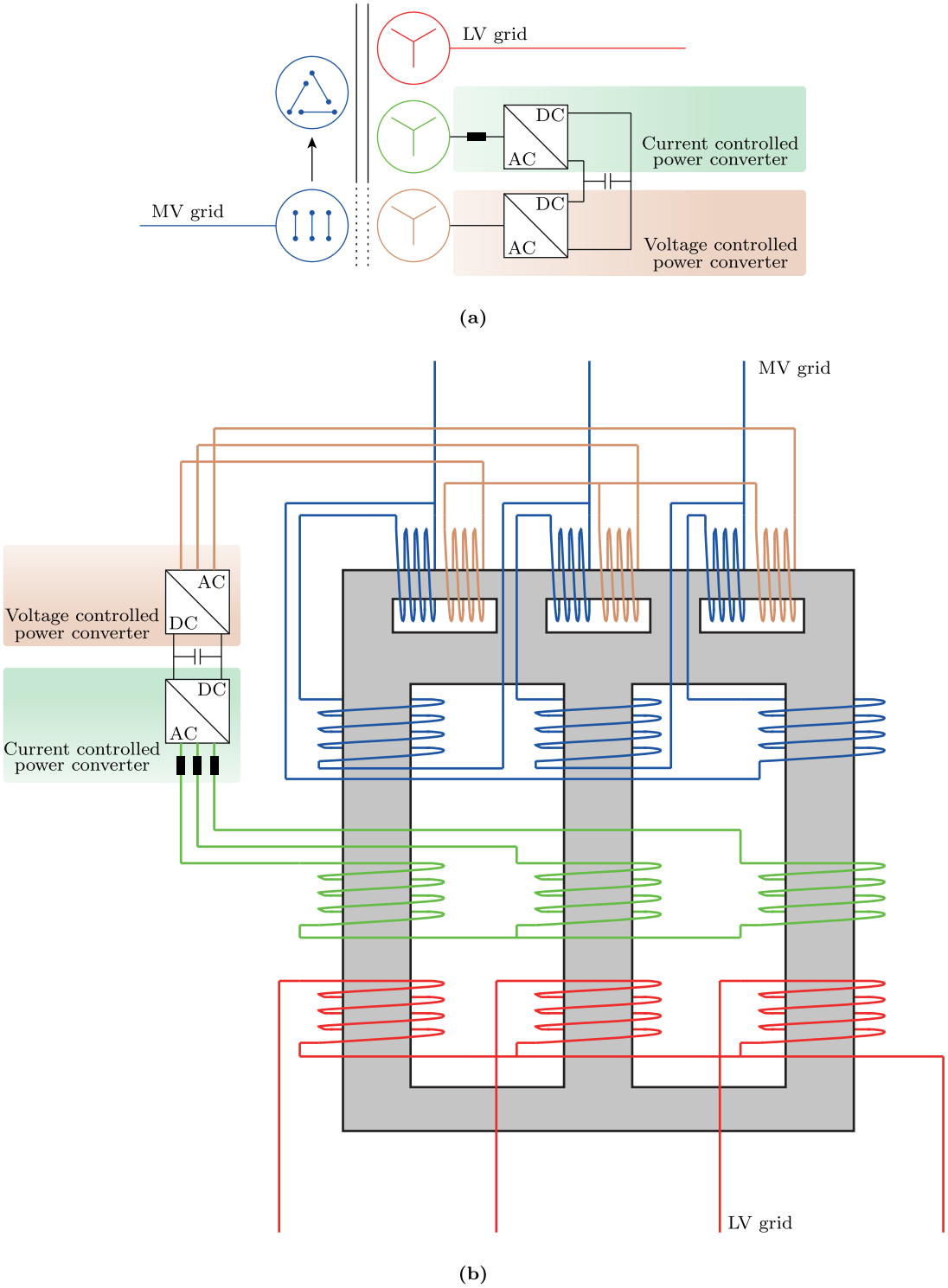
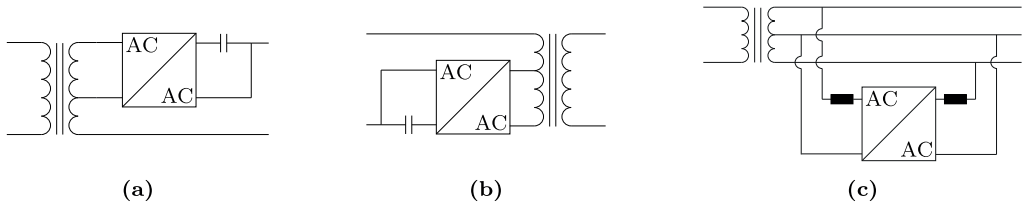


Fig. 1.5. Integrated Magnetics HDT. **(a)** Simplified diagram. **(b)** Winding diagram [64].



(a) (b) (c)

Fig. 1.6. Other HDT configurations. **(a)** Series connection to the high voltage taps. **(b)** Series connection to the low voltage taps. **(c)** Shunt connection to both phases of a single-phase grid with central tap.

indirectly through reactive power injection. A three-phase converter utilizing isolated DC/DC converters is proposed, as well as a single-phase isolated AC/AC converter [70, 71].

1.3.4 Other HDT configurations

In this section, HDT configurations that are less common and do not fit within the previous classification are presented in Fig. 1.6.

In the configuration of Fig. 1.6(a), the power converter is connected to the high-side taps of the LV winding of the LFT. This configuration uses single-phase AC/AC converters per phase, and it was introduced as a controllable network transformer, which can provide power flow control between lines. The nature of the AC chopper converters preserves the input voltage phase without allowing for the modification of the output voltage phase. Nonetheless, utilizing techniques based on harmonics injections, it is possible to shift the fundamental voltage to provide power flow control and act as an active power filter [72,73]. Configuration of Fig. 1.6(b) applies the same idea. The power converter is connected to the neutral-side taps of the MV winding of the LFT. Compared to previous configurations, this solution presents lower conduction losses since the converter is located on the MV side. When utilizing AC chopper converters, switches must commutate between boost and buck mode for sag and swell mitigation, respectively [74]. Alternatively, DC-Link-based converters can be utilized. In this case, the taps-side converter rectifies the tap voltage, and then the end-side converter generates the required AC voltage, injecting it in series to the grid. No switches are required since DC-AC converters can shift their output voltage [75]. In this configuration, load harmonics mitigation is not provided, which can affect and diminish the LFT lifetime.

Finally, the configuration observed in Fig. 1.6(c) is proposed exclusively for LV distribution systems with central tap connection. The power converter is connected between both phases to provide parallel compensation. Additionally, it allows for active

and reactive power sharing between both phases for balancing purposes, reducing the neutral currents [74]. The parallel units can correct the PF and protect the LFT from load harmonics.

1.4 Power converter location effects

The location of the power converter has a decisive role in protecting the LFT, as it can prevent the load and grid voltage harmonics propagation. This is summarized in Fig. 1.7.

1.4.1 Shunt converter location

The power converters connected in parallel configuration can be placed into the MV side, LV side, or AW, as shown in Fig. 1.7(a)–(c), respectively. The different power converter locations share the capability of improving the MV grid PQ by providing, for example, PF correction, harmonics filtering, and neutral current mitigation.

When the parallel converter is placed on the MV side, as seen in Fig. 1.7(a), and in the presence of nonlinear loads, these are not mitigated on the LV side and they are free to flow through the LFT. Distorted currents circulating on the LFT harm the lifetime of the LFT by generating additional losses, acoustic noise, and vibrations. The winding temperature, specifically its hot spot, is a critical variable for LFT as it impacts the winding isolation health. Therefore, the LFT lifetime decreases as no mitigation system is placed on the LV side. One method to deal with harmonic currents on the LFT is transformer derating. Alternatively, suppose the parallel converter is placed on the LV side, as shown in Fig. 1.7(b). In that case, load harmonics can be compensated, preventing their circulation on the LFT and improving the LFT lifetime. Additionally, the connection of the parallel converter on the LV side can be achieved with simple power converter topologies without requiring multilevel alternatives or CTs.

When the power converter is connected to an AW, as in Fig. 1.5, it can provide current regulation by means of the magnetomotive force compensation. Under this scenario, the negative effects of the load currents on the MV side current can be mitigated. Nonetheless, load harmonic currents still circulate through the LV side winding. Moreover, in order to compensate for those currents, the power converter must inject the required compensating harmonics currents into the AW, as represented in Fig. 1.7(c). The compensating currents depend on the load characteristic, the MV and LV winding ratios, and the AW configuration. Although the MV side winding currents are compensated in terms of PQ, the currents circulating through the LV and AW can contain high amounts of harmonics.

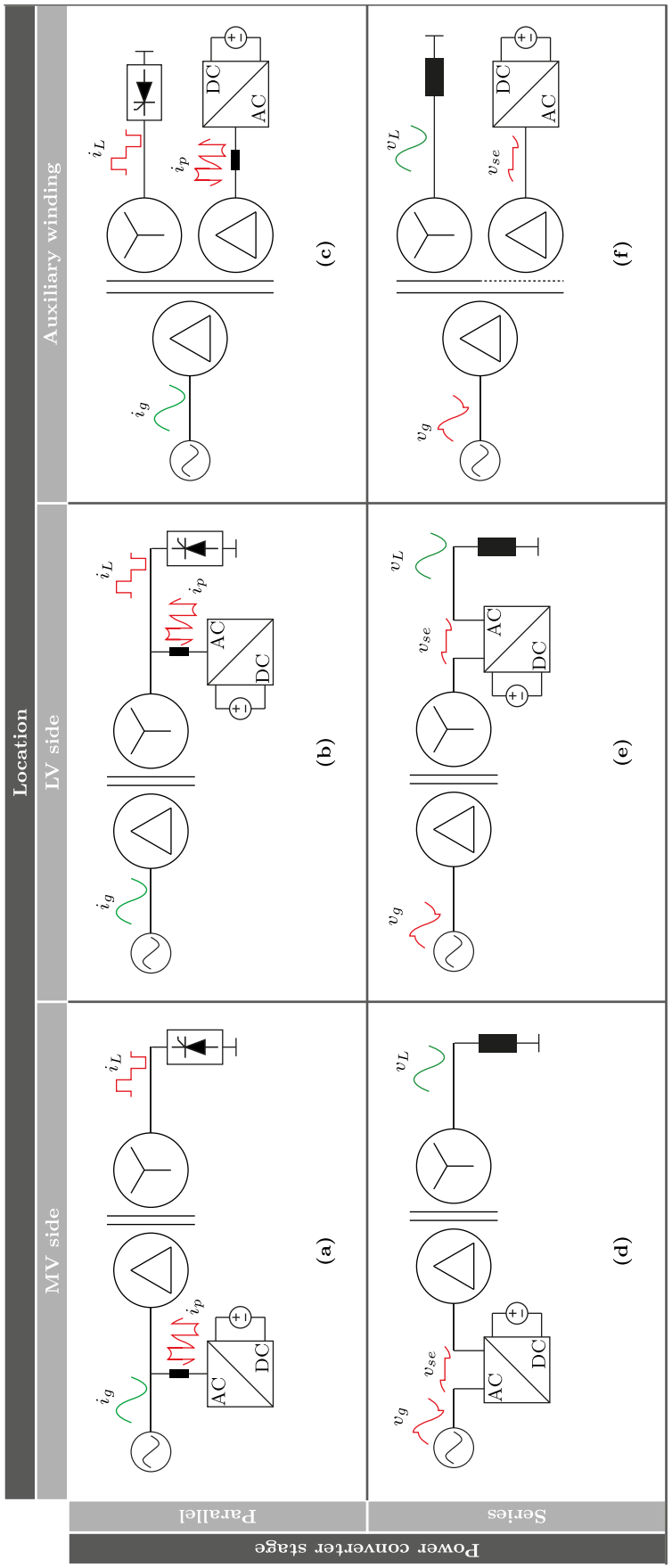


Fig. 1.7. Parallel and series converter locations. **(a)** Parallel converter connected to the MV side. **(b)** Parallel converter connected to the LV side. **(c)** Parallel converter connected to the AW. **(d)** Series converter connected to the MV. **(e)** Series converter connected to the LV side. **(f)** Series converter connected to the AW.

Therefore, the LFT must be designed to operate under these conditions.

1.4.2 Series converter location

Power converters connected in series to the distribution line can mitigate voltage-based PQ problems, such as grid voltage sags, swells, voltage unbalances, and voltage harmonics.

As with the parallel converter, the location of the series converter has a significant impact on the LFT. When the series converter is placed on the MV side, as in Fig. 1.7(d), the supplied voltage to the LFT can be regulated, improving LFT performance and simultaneously controlling the load voltage. The same effect can be obtained if the converter is placed on the LV side, as in Fig. 1.7(e). Nonetheless, the LFT is unprotected from voltage disturbances, which can cause additional losses and inrush currents that can distort the rest of the grid.

An alternative to previous methods consists of connecting the power converter to an AW, as in Fig. 1.7(f) and Fig. 1.5. Depending on the specific magnetic configuration of the LFT, the harmonic voltages from the grid and those injected by the power converter might affect the magnetic core paths associated with their windings. The resultant magnetic flux circulating in the magnetic path associated with the LV side winding will be improved as well as the resultant voltage waveform on the output converter terminals. The magnetic core legs of the MV and AW will be under the stress of disturbed voltage, causing additional core losses. Especially considering nonlinear reluctance, voltage disturbances can cause inrush currents on both circuits.

1.4.3 Combined compensation and circulating active power flow

It is possible to combine the series and shunt converters into one solution, as shown in the configurations of Fig. 1.4(e)–(i). Among these configurations, two groups can be highlighted. Configurations of Fig. 1.4(e)–(f) take their energy from the AW and inject them in series to the distribution line. On the other hand, configurations of Fig. 1.4(h)–(i) take their energy from the LV winding and inject them in series to the grid. In both groups, two scenarios can be studied according to the location of the series converter, i.e., if the series converter is connected to the MV or LV side.

Taking configuration Fig. 1.4(i) as a reference and connecting the series converter on the LV side, the power flow is shown in Fig. 1.8(a). It can be seen that part of the power flow deviates through the power converter stage in order to be processed and later injected in series to the grid.

A feedback phenomenon exists when the CT is connected on the MV side, as

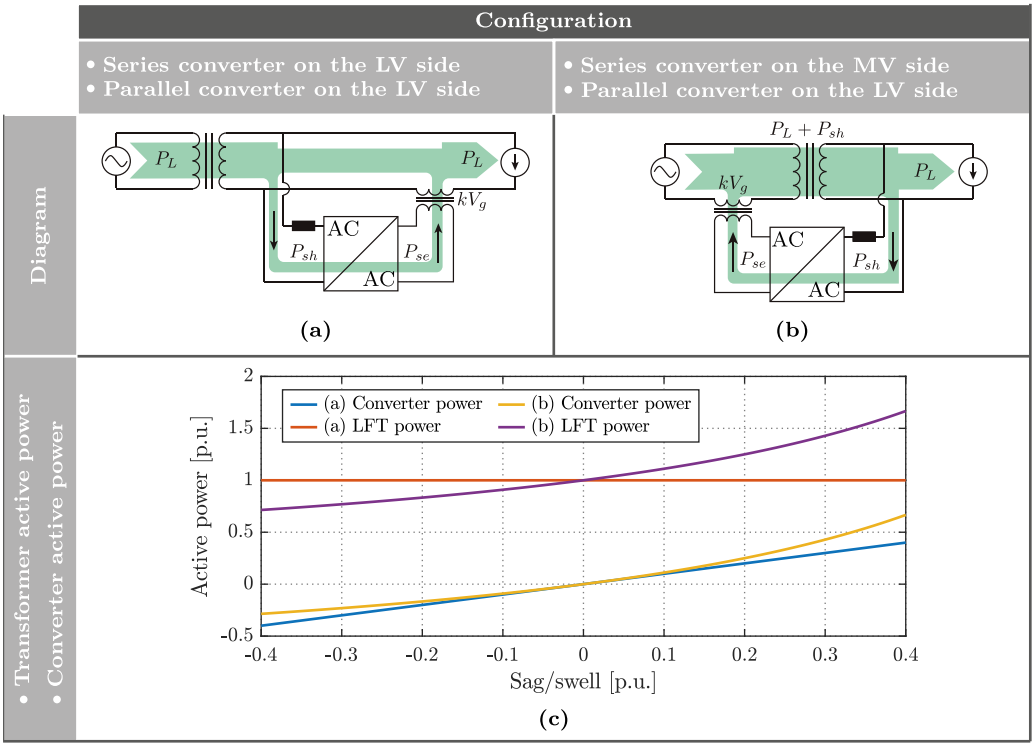


Fig. 1.8. Active power flow scenarios. **(a)** No CAPF between the LFT and the power converter. **(b)** CAPF between the LFT and power converter. **(c)** Power converter and LFT active power.

in Fig. 1.8(b), increasing the power demand through the main LFT. The additional amount of power circulating between the main LFT and power converters is treated as a Circulating Active Power Flow (CAPF) in this work, and a detailed study of this phenomenon is presented in **Chapter 4**.

The CAPF between the LFT and the power converter exists in the presence of a voltage disturbance. In periods of high load, the additional power can overload the LFT, which could affect its lifetime.

Fig. 1.8(c) presents the required injected active power by the power converter in order to compensate for different grid voltage sags, as well as the total amount of active power processed by the LFT for both configurations. These values are calculated assuming the power converter and the LFT are ideal. As expected, the additional power requirements increase as the voltage sags to compensate are higher. If the power converter losses are considered, higher active power values will be required to compensate for voltage sags, decreasing the overall efficiency. Additionally, if the LFT losses and leakage impedances are considered, the additional CAPF required generates additional voltage drops, which the power converter must regulate. Therefore, the power converter must compensate for the grid voltage sag and the voltage drop generated by its operation, representing a higher

equivalent voltage sag, increasing the required CAPF and losses.

1.5 Applications of HDTs

In terms of cost, an HDT is expected to have a higher price than a conventional LFT due to the inclusion of the power converter. Some aspects that will determine the cost of an HDT are the number of power converters considered, i.e., the number of series and parallel converters and the power converter topology. The converter location plays an important role in the costs, as integrating the power converter into the MV is more technically challenging than its LV counterpart. The latter requires the use of multilevel power converters or MV protections and isolators. Beyond the cost of the power converter, the additional services that the HDT can provide make it an interesting alternative for electrical companies.

Besides the previously mentioned capabilities of an HDT, such as current and voltage harmonic filtering, PF correction, voltage regulation, load balancing, and neutral current mitigation, additional applications of HDTs have been researched, and are summarized in Fig. 1.9. The provided service and its impact on the grid or distribution transformer will depend on the selected HDT configuration and topology. Some of these services are presented in the following subsections.

1.5.1 Distribution transformer inrush current mitigation

There are several methods to reduce the impact of inrush currents at the moment of the distribution transformer connection, for example, by connecting the transformer phases in sequences at optimal moments. Nonetheless, it is possible to use the parallel stage of HDTs to mitigate their impact. Based on Fig. 1.9(a), and using a prefluxing technique, the power converter induces a magnetic flux equal to that induced by the grid at the connection instant, reducing the generation of inrush currents. Once the transformer is connected to the grid, the power converter can be synchronized to the LV side to initiate its normal operation, regulating the LV side voltages and currents. When it is desired to disconnect the transformer, the same technique is applied, but in the reverse order, until the transformer flux is zero. This feature is proposed utilizing the configuration of Fig. 1.4(e) along with a DC storage system connected to the DC-Link to provide the necessary energy to magnetize the transformer [76].

Alternatively, the same configuration can be applied to reduce magnetizing flux DC offsets, which generate inrush currents. The mitigation is carried out by the power

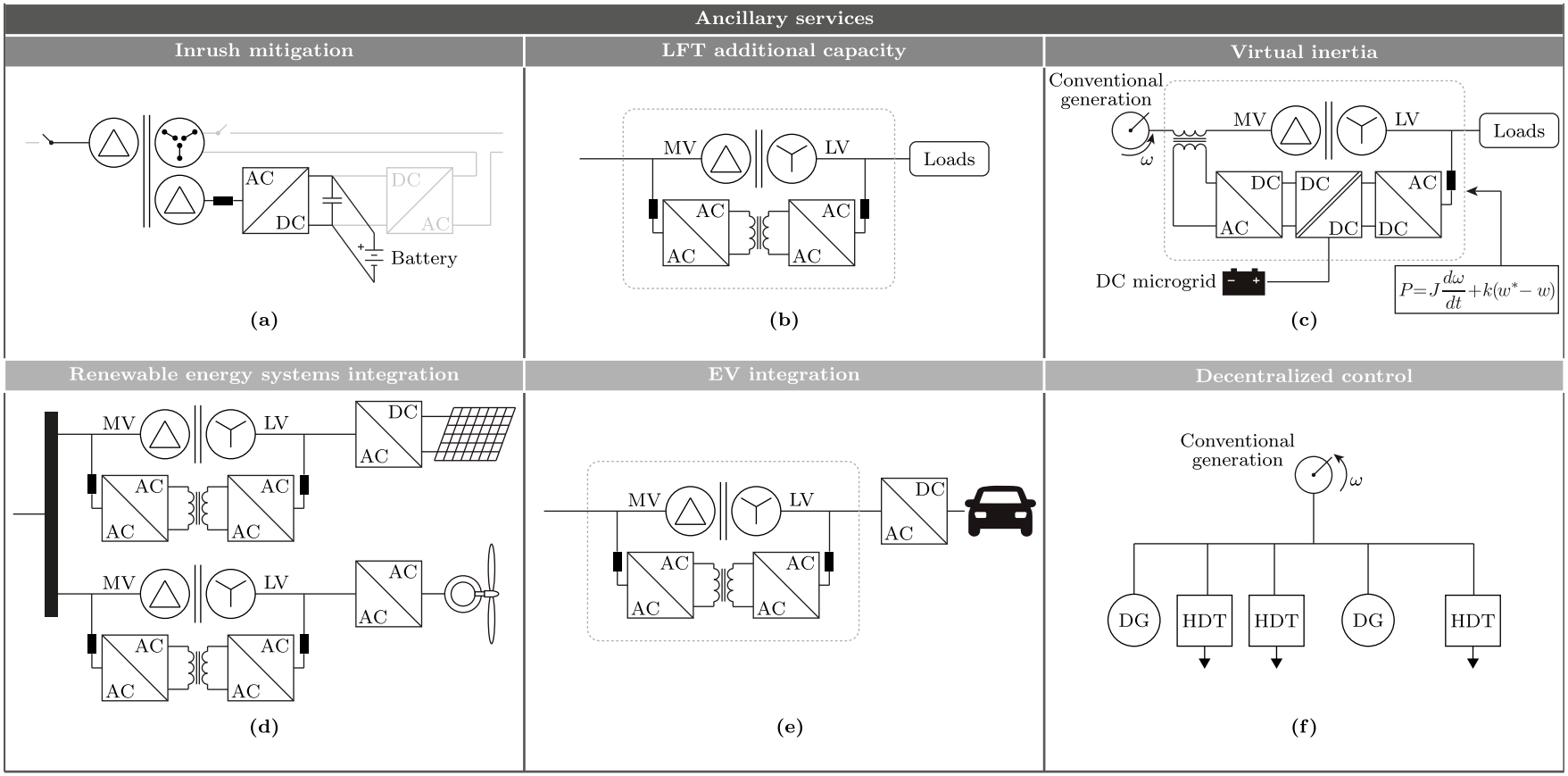


Fig. 1.9. Ancillary services provided by HDTs. **(a)** inrush current mitigation. **(b)** Increase in an LFT capacity by means of an HDT. **(c)** HDT to provide virtual inertia. **(d)** Renewable systems integration. **(e)** Electric vehicle charging station. **(f)** Voltage regulation of an ADN by means of HDTs.

converter module connected to the AW, modifying the core flux [77].

1.5.2 Distribution transformer additional capacity

By means of a parallel connection of a power converter isolated with HFTs, such as the configuration of Fig. 1.4(j), and by utilizing active and reactive power control, it is possible to increase the capacity of an LFT. This scenario is represented in Fig. 1.9(b). The power control is designed to supply a proportion of the load while providing PQ mitigation services. Proposed solutions integrate a full-rated power converter parallel to the conventional transformer [71, 78, 79].

1.5.3 HDTs to provide virtual inertia

In HDT with DC ports, it is possible to employ BESS or distributed generation systems to provide grid frequency support. This solution is attractive in low-mechanical inertia grids, where HDTs can be exploited [80]. Additionally, if multiple units are employed in a power system, their impact can be significantly improved. Fig. 1.9(c) shows the DC system integration to the DC-Link of the HDT to provide grid frequency support.

An external control loop can improve the grid inertia, which allows the softening of the frequency dynamic behavior under contingencies, providing primary frequency support. The control is based on modifying the converter injected power according to the grid frequency variation, emulating the synchronous generator mechanical equation [81, 82].

1.5.4 Renewable energy systems and new kind of loads integration

Conventional transformers can integrate PV or wind generation systems into the grid. Their electromagnetic characteristic significantly impacts PQ, especially during low radiation and wind speed periods in weak grids. This operating scenario is translated into a low active power injection by the renewable generating units and makes the magnetizing transformer currents considerable with respect to load currents. The generated harmonics by this phenomenon mainly depend on the winding connection type and the harmonic content presented on the grid voltage [70].

Fig. 1.9(d) shows the presented scenario employing an HDT, which uses the configuration of Fig. 1.4(j). It allows for attenuating the impact of the renewable systems on the power electric system through an appropriate control system, which accounts for the transformer currents in the model. By doing this, the grid current on the MV side

is proportional to the current injected by the renewable generating units for all radiation and wind speed ranges. Additionally, it is possible to design the controllers to operate with unit PF if the converter rating allows it [70].

New kinds of loads, such as electric vehicles, can produce additional stress on distribution transformers, for instance, during multiple charging processes occurring in the evening and night-time, especially at the domiciliary level [16]. Using an HDT, as exemplified in Fig. 1.9(e), can benefit the LFT lifetime, as the power converter can dampen the power consumption and avoid overloading the LFT.

1.5.5 Decentralized control of an HDT for voltage regulation in active grids

Expanding the use of distributed generation represents a challenge for the planning of distribution grids. One of the main concerns is the effect of the intermittence of renewable sources, which for example impacts the voltage profile of the distribution grid. Therefore, using smart devices and new control techniques is required to cope with these challenges.

Active Distribution Networks (ADNs) can take advantage of HDTs in order to improve the voltage profiles. For example, the HDT configuration of Fig. 1.4(e) can provide voltage control to the LV side by means of the series converter. On the other hand, the power converter connected to the AW can absorb/inject a limited amount of reactive power, which, in conjunction with other HDTs or smart devices, can provide voltage regulation to the MV buses.

Multiple HDTs, as shown in Fig. 1.9(f), can be coordinated to regulate the voltage magnitude of the MV buses while optimizing the reactive power injection/consumption of the HDTs. This task can be done in a decentralized manner, utilizing HDTs controlled with local variables exclusively [83].

1.6 Thesis motivation

There are multiple HDT configurations proposed in the literature, as well as power converter topologies applied to it [38]. Selected configurations are presented in Fig. 1.10. The most recurrent configuration is based on a parallel converter connected to an AW of the LFT, and a series converter connected to the LV grid, as Fig. 1.10(a) shows [84]. It provides continuous voltage regulation to the load, while the current-controlled stage establishes the DC-Link and provides PF correction. No CTs are required in this configuration.

	Configuration		
	(a)	(b)	(c)
Advantages	• No CTs • No circulating active power flow	• Full isolation • Magnetic integration LFT + CTs	• Retrofitting • Sinusoidal currents on LFT • Sinusoidal voltage on LFT
Disadvantages	• No retrofitting • Low voltage - High current power converters (Interleaved) • Nonlinear currents on LFT windings • Nonlinear voltages on LFT windings	• No retrofitting • Nonlinear currents on LFT windings • Circulating active power flow • CTs required	• Circulating active power flow • CTs mandatory (Isolation primary - secondary)

Fig. 1.10. Qualitative comparison of HDT configurations. **(a)** Power converter connected to AWs and in series without CTs. **(b)** Power converter connected to AWs and in series with CT. **(c)** Power converter connected to the LV side and in series with CTs.

An alternative configuration is presented in Fig. 1.10(b) [85]. The current-controlled power converter is connected to the AW of the LFT, but the series converter is integrated into the MV grid. The AWs and the CTs isolate the power converter from the distribution grid, which benefits its safety. Additionally, the turn number of both windings adds degrees of freedom to the HDT design, allowing optimization. Moreover, an additional degree of optimization is possible by doing the magnetic integration between the LFT and the CTs [86].

The previous HDT configurations require the presence of AWs to connect the shunt converter. In cases where the power converters are used to provide PF correction and/or load current active filtering, the load and compensating currents will flow through the LV winding and AWs, respectively [87]. This process increases the copper losses of the HDT. Therefore, the LFT must be designed to operate under these conditions, requiring K-rated transformers [21,88]. The additional and bigger winding will negatively affect the weight of the LFT, its mounting structure, and, consequently, the cost. Moreover, due to the requirement of the AW, no retrofitting is possible for conventional LFTs in operation. On the other hand, in terms of power converters, the solution provided in Fig. 1.10(a) operates at a fraction of the LV side voltage. Therefore, low voltage and very high currents power converters are necessary, which would require interleaved configurations.

Considering the issues of the previous HDTs, this work proposes a configuration in which the power converters are connected to the MV and LV sides would improve the PQ on the distribution grid and extend the LFT lifetime. This configuration is shown in Fig. 1.10(c). The use of CTs is mandatory in order to maintain the isolation between the MV and LV sides, and due to the connection to the LV grid, conventional LV power converters can be utilized. The series converter connected to the MV side can regulate the load voltage and protect the LFT from grid voltage disturbances that could generate high-amplitude currents and mitigate supply voltage harmonics that could affect the LFT operation. Due to the location of the series converter, the load voltage can be regulated and kept around its rated value [89]. Therefore, in the presence of under and overvoltages, the shunt converter can continue its operation without exceeding its connection point voltage limits. On the other hand, the parallel converter on the LV side can improve the current quality through the LFT and extend its lifetime [8, 90]. The proposed configuration has the advantage of being able to be applied to existing LFTs in operation, allowing retrofitting.

1.7 Formulation of the thesis

This thesis is devoted to the investigation of a specific HDT configuration in which the series converter is connected to the MV side through CTs, and the parallel converter is directly connected to the LV side. The following thesis can be formulated:

"The novel Hybrid Distribution Transformer configuration and control algorithm improve the grid and load power quality under varying conditions, as well as enable the better operation conditions of its main Low-Frequency Transformer"

In order to prove the above thesis, the author used an analytical and simulation-based approach, as well as simulation and experimental verification with a laboratory setup.

1.8 Contributions of the author

In the opinion of the author, the following corresponds to his original contribution:

- A HDT configuration with a series/parallel converter on the MV/LV side.
- Mathematical and simulation models of the proposed HDT for the different studied operating conditions.
- A discrete-time control algorithm to improve the PQ on the main transformer, grid, and load.
- Modelling and experimental verification of the losses and CAPF model of the proposed HDT.
- Proposal and applicability of two methods to reduce the CAPF.
- Proposal of a control algorithm for the improvement of the flux of the main transformer of the HDT.
- Development of an experimental setup of the proposed HDT and experimental validation of the thesis.

1.9 Outline of the dissertation

This thesis consists of six chapters, which are organized as follows.

Chapter 1 introduces the problem with the actual distribution systems, and the requirements of modern power systems. The HDT is reviewed and the thesis is described.

Chapter 2 presents the model of the HDT, which will be later utilized as a base in the remainder of the dissertation. For the series converter, a LC type filter is utilized, whereas for the parallel a LCL is employed. The low-voltage grid corresponds to both 3-wire and 4-wire configurations.

Chapter 3 presents the operation of the HDT under balanced conditions, using a controller system based on the dq frame. In this chapter, the stability of the HDT is assessed considering the interaction given by the LC and LCL circuits. The CAPF is observed.

Chapter 4 is devoted to the study of the CAPF. For this means, the unbalanced operation of the HDT is taken into consideration, neglecting the load and grid harmonics pollution. The control of the HDT for unbalanced conditions is presented, and methods to reduce the CAPF are introduced.

Chapter 5 is focused on the application of the HDT to improve the PQ of the distribution grid, considering a 3-wire and 4-wire distribution grid.

Chapter 6 serves as a proof of concept of the application of the HDT to regulate the flux of the main LFT during voltage sags and swells in order to avoid inrush currents.

1.10 Publications generated from the doctoral thesis

The following journal and international conference publications were derived from the work of this thesis.

1.10.1 Journal publications

[1] A. Carreno, M. Malinowski and M. A. Perez, "Circulating Active Power Flow Analysis in Hybrid Transformers," in Early Access of *IEEE Transactions on Industrial Electronics*, January 2024.

[2] A. Carreno, M. A. Perez and M. Malinowski, "State-Feedback Control of a Hybrid Distribution Transformer for Power Quality Improvement of a Distribution Grid," in *IEEE Transactions on Industrial Electronics*, vol. 71, no. 2, pp. 1147-1157, Feb. 2024

[3] Carreno, A.; Perez, M.; Baier, C.; Huang, A.; Rajendran, S.; Malinowski, M. Configurations, "Power Topologies and Applications of Hybrid Distribution Transformers". *Energies*, 2021, 14, 1215.

1.10.2 International conference publications

[1] A. Carreno, M. Malinowski, and M. A. Perez, "Stability Analysis of a Hybrid Distribution Transformer with a Series/Parallel Converter Connected to the Primary/Secondary Side", *2024 4th International Conference on Smart Grid and Renewable Energy (SGRE)*, Doha, Qatar, 2024, pp. 1-6, **Best paper award**.

[2] A. Carreno, M. Malinowski, and M. A. Perez, "Circulating Active Power Flow and DC-Link Voltage Ripple in Hybrid Transformers", *IECON 2023 The 49th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, 2023, pp. 1-6.

[3] A. Carreno, M. A. Perez , and M. Malinowski, "Flux Compensation in a Hybrid Transformer with the Series Converter Connected on the Primary-Side", *2023 IEEE 17th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, Tallin, Estonia, 2023, pp. 1-6.

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Chapter 2

MODEL OF THE HDT

This chapter presents the mathematical model of the HDT with the series converter connected to the MV side and the parallel converter connected to the LV side of the main LFT. The proposed HDT is presented, which is divided into two main subsystems:

1. A series power converter with an LC filter on its output.
2. A parallel power converter with an LCL filter on its output.

Both systems are interconnected through the main LFT and the DC-Link. Then, the open-loop dynamic model of each component and the combined model are presented. The problem regarding the interaction of both systems is introduced.

Note about nomenclature

When referring to a general three-phase variable, x, the following nomenclature will be used:

- x_{abc}: Vector containing three-phase quantities.
- x_{abcn}: Vector containing three-phase quantities including the neutral component.
- x_a, x_b, x_c, x_n: The individual components of the vectors x_{abc} or x_{abcn}.

- $x_{\alpha\beta\gamma}$: A vector containing the α, β, and γ components of x_{abc} or x_{abcn}.
- $x_{\alpha\beta}$: A vector containing the α and β components of x_{abc} or x_{abcn}
- x_{α}, x_{β}, x_{γ}: The individual components of $x_{\alpha\beta\gamma}$.

2.1 System under study

The HDTs utilized in this work are shown in Fig. 2.3. The HDTs for three-phase distribution grids with and without neutral wire are shown in Fig. 2.3(a)–(b), respectively. Conventional two-level power converters are utilized in both cases, and a 4-leg power converter is employed for the 4-wire distribution. The main LFT has a $\Delta - Y$ configuration with a turns ratio equal to N_{sp}.

A voltage-controlled power converter using an LC filter is connected in series to the primary side through CTs with a turns ratio equal to N_{se}. The filter inductance and capacitance correspond to L_1 and C_1, respectively. The task of this converter is to mitigate the disturbances presented in the grid voltage, v_g, and therefore improve the voltage quality on the terminals of the LFT, balancing and improving the power quality of the LV side, v_2.

On the other hand, the parallel power converter is connected to the LV side of the main LFT, forming an LCL filter with the equivalent series impedance of the LFT. L_2 correspond to the converter inductance, C_2 is the output filter capacitance, and L_s corresponds to the equivalent leakage impedance of the LFT. This converter regulates the DC-Link voltage, v_{dc}, improves the PF, and balances the load current, i_L, to improve the quality of the secondary current, i_s. The DC-Link capacitance is C_{dc}.

In this chapter, the model of the LFT and CTs are considered to be linear, neglecting their magnetizing branches. For the CTs, the equivalent series impedance is also neglected. Nonetheless, in **Chapter 4**, the effect of the series impedances and equivalent core losses are considered to analyze the power flow and efficiency of the HDT.

2.2 Series converter model

For both HDTs presented in Fig. 2.1, the circuit corresponding to the series converter is shown in Fig. 2.2. in which the CTs are not considered for now. The output current of the power converter, i_1, is modeled by the following equation:

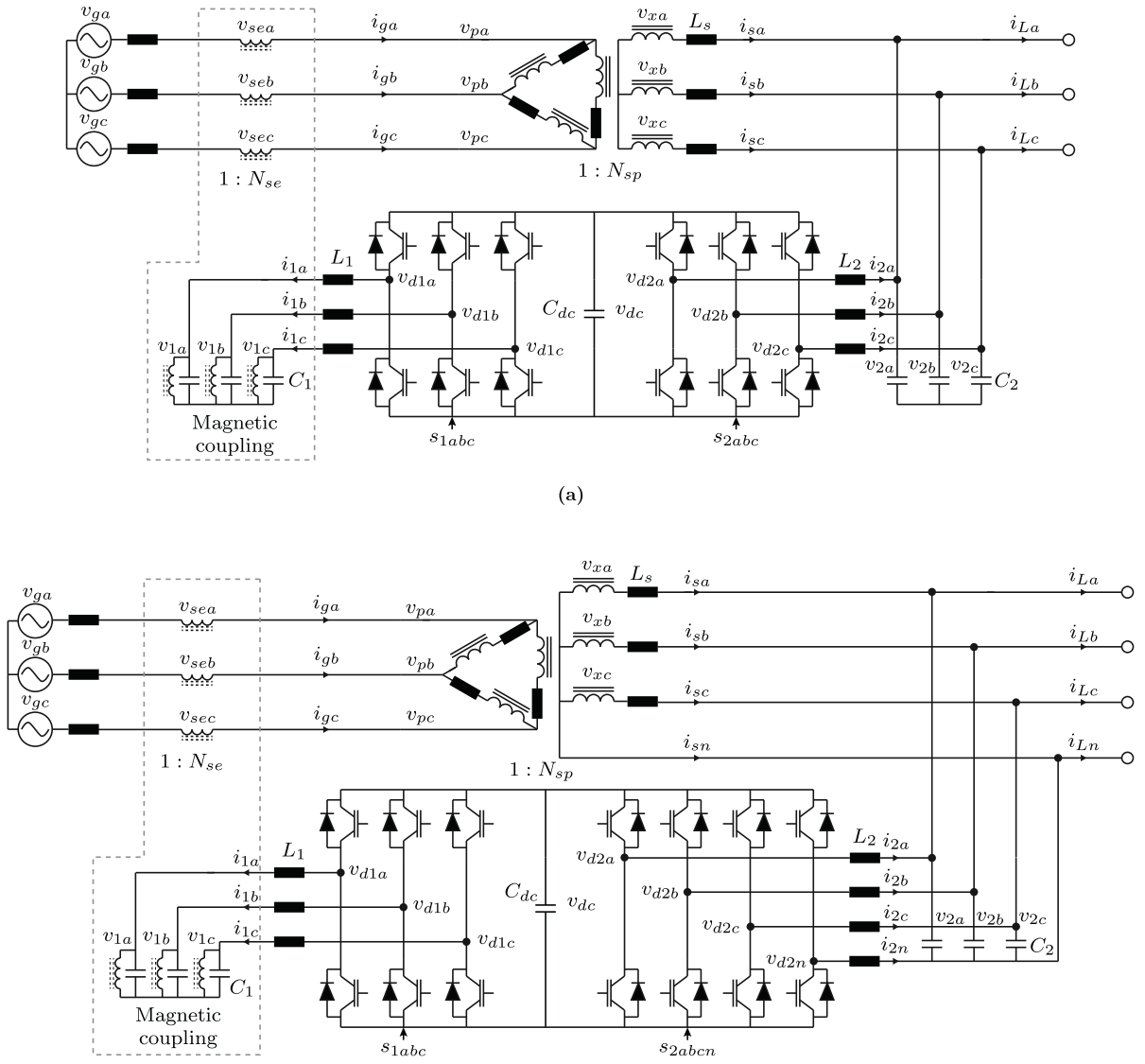


Fig. 2.1. Proposed HDT configuration with a series converter on the MV side and a parallel converter on the LV side. **(a)** Three-wire low-voltage distribution grid. **(b)** Four-wire low-voltage distribution grid.

$$L_1 \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \end{bmatrix} = -R_1 \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \end{bmatrix} + \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{d1a} \\ v_{d1b} \\ v_{d1c} \end{bmatrix} - \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} \tag{2.2.1}$$

where v_{d1} is the voltage on the power converter terminals, and v_1 is the LC filter capacitor

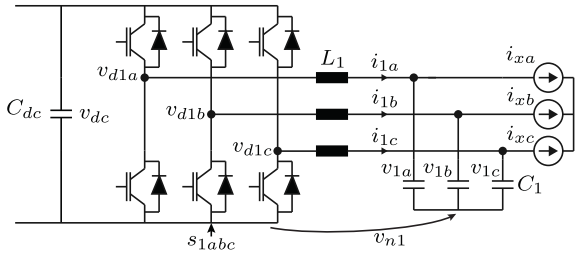


Fig. 2.2. Series converter with output LC filter.

voltage. The previous model is obtained considering that the common-mode voltage between the power converter and the capacitor bank neutral points, v_{n1}, is given as follows.

$$v_{n1} = \frac{(v_{d1a} + v_{d1b} + v_{d1c}) - (v_{1a} + v_{1b} + v_{1c})}{3} \tag{2.2.2}$$

The capacitor voltage is the output of this subsystem, which then, through the CTs, is transferred and injected in series to the grid to provide voltage regulation. The capacitor voltage is mathematically represented as follows.

$$C_1 \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} = -\frac{1}{R_{c1}} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} + \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \end{bmatrix} - \begin{bmatrix} i_{xa} \\ i_{xb} \\ i_{xc} \end{bmatrix} \tag{2.2.3}$$

where i_x corresponds to the current that circulates on the primary side of the CTs. This variable corresponds to the grid current reflected in the subsystem of the series converter.

The equations that model the LC filter, (2.2.1) and (2.2.3), can be transformed into the $\alpha\beta\gamma$ coordinates system utilizing the following transformation matrix.

$$\mathbf{T}_{\alpha\beta\gamma} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.2.4}$$

There are no common-mode currents and voltages due to the open neutral configuration. Therefore the γ component is neglected. Then, the inductor current and capacitor voltage in $\alpha\beta$ coordinates are grouped into a single state vector, $x_{1\alpha\beta}$, which is defined as follows.

$$x_{1\alpha\beta} = \begin{bmatrix} v_{1\alpha\beta} \\ i_{1\alpha\beta} \end{bmatrix} \tag{2.2.5}$$

Then, considering the previous equation, the following equation models the LC filter in its state-space representation.

$$\dot{x}_{1\alpha\beta} = \mathbf{A_{c1}} x_{1\alpha\beta} + \mathbf{B_{c1}} v_{d1\alpha\beta} + \mathbf{P_{c1}} i_{x\alpha\beta} \tag{2.2.6}$$

in which the controlled input of the system corresponds to the output voltage of the parallel converter, $v_{d1\alpha\beta}$, and the system disturbance is the current that circulates through the primary winding of the coupling transformer, $i_{x\alpha\beta}$. The matrices $\mathbf{A_{c1}}$, $\mathbf{B_{c1}}$, and, $\mathbf{P_{c1}}$ are defined below.

$$\mathbf{A_{c1}} = \begin{bmatrix} -1/R_{c1}C_1\mathbf{I} & 1/C_1\mathbf{I} \\ -1/L_1\mathbf{I} & -R_1/L_1\mathbf{I} \end{bmatrix} \tag{2.2.7a}$$

$$\mathbf{B_{c1}} = \begin{bmatrix} \mathbf{O} \\ 1/L_1\mathbf{I} \end{bmatrix} \tag{2.2.7b}$$

$$\mathbf{P_{c1}} = \begin{bmatrix} -1/C_1\mathbf{I} \\ \mathbf{O} \end{bmatrix} \tag{2.2.7c}$$

where the matrices $\mathbf{I}$ and $\mathbf{O}$ are the $2x2$ identity and zero matrices.

$$\mathbf{I} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{2.2.8a}$$

$$\mathbf{O} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{2.2.8b}$$

The outputs of the system correspond to each one of the state variables, and they are given by the following equations.

$$v_{1\alpha\beta} = \mathbf{C_{1v1}} x_{1\alpha\beta} \tag{2.2.9a}$$

$$i_{1\alpha\beta} = \mathbf{C_{1i1}} x_{1\alpha\beta} \tag{2.2.9b}$$

where $\mathbf{C_{1v1}}$ and $\mathbf{C_{1i1}}$ are the following matrices.

$$\mathbf{C_{1v1}} = \begin{bmatrix} \mathbf{I} & \mathbf{O} \end{bmatrix} \tag{2.2.10a}$$

$$\mathbf{C_{1i1}} = \begin{bmatrix} \mathbf{O} & \mathbf{I} \end{bmatrix} \tag{2.2.10b}$$

The previous equations model the LC filter of the series converter in $\alpha\beta$ coordinates in its state-space representation.

2.3 Parallel converter model

The 4-leg parallel converter is a generalized topology of the 3-leg alternative. Therefore, in this chapter, the 4-leg converter will be considered for modeling purposes. Later, the model will be written in terms of its $\alpha\beta\gamma$ components. For both power converter topologies, the $\alpha\beta$ components are identical, and they are only differentiated by the γ component, which does not appear in the 3-leg converter.

The diagram of the 4-wire parallel converter is presented in Fig. 2.3. Considering the load is a disturbance, and the induced voltage on the LV side is a voltage source, the system can be treated as a power converter with an LCL filter on its output.

The output current of the parallel power converter, i_2, is modeled by the following equations.

$$L_2 \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{2a} \\ i_{2b} \\ i_{2c} \end{bmatrix} = -R_2 \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \begin{bmatrix} i_{2a} \\ i_{2b} \\ i_{2c} \end{bmatrix} + \begin{bmatrix} v_{d2a} - v_{d2n} \\ v_{d2b} - v_{d2n} \\ v_{d2c} - v_{d2n} \end{bmatrix} - \begin{bmatrix} v_{2a} \\ v_{2b} \\ v_{2c} \end{bmatrix} \tag{2.3.1}$$

where v_{d2} is the voltage on the power converter terminals, v_2 is the LCL capacitor voltage. The neutral voltage of the 4-leg power converter, v_{d2n}, appears as a common-mode voltage. On the other hand, the secondary-side current of the HDT, i_s, is represented by the following equations.

$$L_s \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = -R_s \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} + \begin{bmatrix} v_{xa} \\ v_{xb} \\ v_{xc} \end{bmatrix} - \begin{bmatrix} v_{2a} \\ v_{2b} \\ v_{2c} \end{bmatrix} \tag{2.3.2}$$

where v_x is the voltage induced in the main LFT terminals. v_x has no common-mode component because it is eliminated by the $\Delta - Y$ transformer. Then, the dynamic

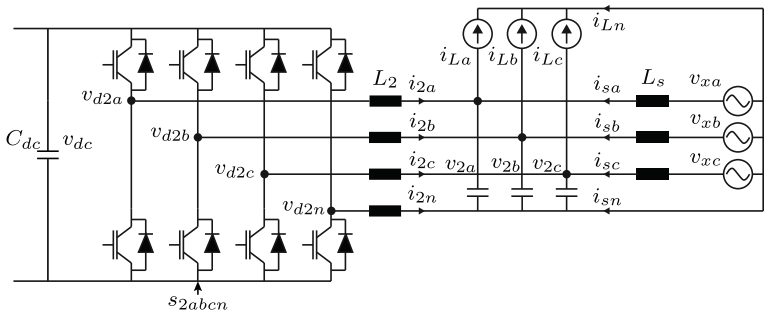


Fig. 2.3. Parallel converter of the HDT.

equations of the capacitor voltage are written as follows.

$$C_2 \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} v_{2a} \\ v_{2b} \\ v_{2c} \end{bmatrix} = -\frac{1}{R_{c2}} \begin{bmatrix} v_{2a} \\ v_{2b} \\ v_{2c} \end{bmatrix} + \begin{bmatrix} i_{2a} \\ i_{2b} \\ i_{2c} \end{bmatrix} + \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} - \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{2.3.3}$$

where i_L is the load current, which is modeled as a current source. The neutral currents are given by the following equations.

$$i_{2n} = -(i_{2a} + i_{2b} + i_{2c}) \tag{2.3.4a}$$
$$i_{sn} = -(i_{sa} + i_{sb} + i_{sc}) \tag{2.3.4b}$$
$$i_{Ln} = -(i_{La} + i_{Lb} + i_{Lc}) \tag{2.3.4c}$$

2.3.1 State-space representation in $\alpha\beta$ coordinates

This section presents the model of the LCL filter in its state-space in $\alpha\beta$ coordinates. The transformation matrix of (2.2.4) is applied to the dynamic models of (2.3.1), (2.3.2), and (2.3.3), and then the models are combined in a single matrix representation as follows.

$$\dot{x}_{2\alpha\beta} = \mathbf{A_{c2}} x_{2\alpha\beta} + \mathbf{B_{c2}} v_{d2\alpha\beta} + \mathbf{P_{c2v}} v_{x\alpha\beta} + \mathbf{P_{c2i}} i_{L\alpha\beta} \tag{2.3.5}$$

where $x_{2\alpha\beta}$ is the state vector of the LCL filter.

$$x_{2\alpha\beta} = \begin{bmatrix} i_{2\alpha\beta} \\ i_{s\alpha\beta} \\ v_{2\alpha\beta} \end{bmatrix} \tag{2.3.6}$$

The controlled input of the system corresponds to the output voltage of the parallel converter, $v_{d2\alpha\beta}$. In contrast, the disturbances are the load current, $i_{L\alpha\beta}$, and the equivalent induced voltage on the LV side, $v_{x\alpha\beta}$. The matrices $\mathbf{A_{c2}}$, $\mathbf{B_{c2}}$, $\mathbf{P_{c2v}}$, and $\mathbf{P_{c2i}}$ are shown below.

$$\mathbf{A_{c2}} = \begin{bmatrix} -R_2/L_2\mathbf{I} & \mathbf{O} & -1/L_2\mathbf{I} \\ \mathbf{O} & -R_s/L_s\mathbf{I} & -1/L_s\mathbf{I} \\ 1/C_2\mathbf{I} & 1/C_2\mathbf{I} & -1/R_{c2}C_2\mathbf{I} \end{bmatrix} \tag{2.3.7a}$$

$$\mathbf{B_{c2}} = \begin{bmatrix} 1/L_2\mathbf{I} \\ \mathbf{O} \\ \mathbf{O} \end{bmatrix} \tag{2.3.7b}$$

$$\mathbf{P_{c2v}} = \begin{bmatrix} \mathbf{O} \\ 1/L_s\mathbf{I} \\ \mathbf{O} \end{bmatrix} \quad \mathbf{P_{c2i}} = \begin{bmatrix} \mathbf{O} \\ \mathbf{O} \\ -1/C_2\mathbf{I} \end{bmatrix} \tag{2.3.7c}$$

The outputs of the system correspond to each one of the state variables, and they are given by the following equations.

$$i_{2\alpha\beta} = \mathbf{C_{2i2}} x_{2\alpha\beta} \tag{2.3.8a}$$

$$i_{s\alpha\beta} = \mathbf{C_{2is}} x_{2\alpha\beta} \tag{2.3.8b}$$

$$v_{2\alpha\beta} = \mathbf{C_{2v2}} x_{2\alpha\beta} \tag{2.3.8c}$$

where $\mathbf{C_{2i2}}$, $\mathbf{C_{2is}}$, and $\mathbf{C_{2v2}}$ are the following matrices.

$$\mathbf{C_{2i2}} = \begin{bmatrix} \mathbf{I} & \mathbf{O} & \mathbf{O} \end{bmatrix} \tag{2.3.9a}$$

$$\mathbf{C_{2is}} = \begin{bmatrix} \mathbf{O} & \mathbf{I} & \mathbf{O} \end{bmatrix} \tag{2.3.9b}$$

$$\mathbf{C_{2v2}} = \begin{bmatrix} \mathbf{O} & \mathbf{O} & \mathbf{I} \end{bmatrix} \tag{2.3.9c}$$

The previous equations model the state-space representation of the LCL filter of the parallel converter in $\alpha\beta$ coordinates.

2.3.2 State-space representation in γ coordinate

The following model is only valid for the 4-wire system, in which the common-mode current exists. After applying the transformation matrix of (2.2.4) to the dynamic models of (2.3.1), (2.3.2), and (2.3.3), the following is obtained once extracting the γ component.

$$\dot{x}_{2\gamma} = \mathbf{A}^{\gamma}_{\mathbf{c2}} x_{2\gamma} + \mathbf{B}^{\gamma}_{\mathbf{c2}} (v_{d2\gamma} - v_{d2n}) + \mathbf{P}^{\gamma}_{\mathbf{c2i}} i_{L\gamma} \tag{2.3.10}$$

where $x_{2\gamma}$ is the state vector of the LCL filter. The γ component of the induced voltage of the transformer is not included in the model because the winding configuration eliminates it.

$$x_{2\gamma} = \begin{bmatrix} i_{2\gamma} \\ i_{s\gamma} \\ v_{2\gamma} \end{bmatrix} \tag{2.3.11}$$

The controlled input of the system corresponds to the difference of the γ component of the converter output voltage and the neutral leg voltage, $v_{d2\gamma} - v_{d2n}$. In contrast, the disturbance is the common-mode load current, $i_{L\gamma}$. The matrices $\mathbf{A}^{\gamma}_{\mathbf{c2}}$, $\mathbf{B}^{\gamma}_{\mathbf{c2}}$, and $\mathbf{P}^{\gamma}_{\mathbf{c2i}}$ are shown below.

$$\mathbf{A}^{\gamma}_{\mathbf{c2}} = \begin{bmatrix} -R_2/4L_2 & 0 & -1/4L_2 \\ 0 & -R_s/L_s & -1/L_s \\ 1/C_2 & 1/C_2 & -1/R_{c2}C_2 \end{bmatrix} \tag{2.3.12a}$$

$$\mathbf{B}^{\gamma}_{\mathbf{c2}} = \begin{bmatrix} 1/4L_2 \\ 0 \\ 0 \end{bmatrix} \tag{2.3.12b}$$

$$\mathbf{P}^{\gamma}_{\mathbf{c2i}} = \begin{bmatrix} 0 \\ 0 \\ -1/C_2 \end{bmatrix} \tag{2.3.12c}$$

The outputs of the system correspond to each one of the state variables, and they are given by the following equations.

$$i_{2\gamma} = \mathbf{C}^{\gamma}_{\mathbf{2i2}} x_{2\gamma} \tag{2.3.13a}$$

$$i_{s\gamma} = \mathbf{C}^{\gamma}_{\mathbf{2is}} x_{2\gamma} \tag{2.3.13b}$$

$$v_{2\gamma} = \mathbf{C}^{\gamma}_{\mathbf{2v2}} x_{2\gamma} \tag{2.3.13c}$$

where $\mathbf{C}^{\gamma}_{\mathbf{2i2}}$, $\mathbf{C}^{\gamma}_{\mathbf{2is}}$, and $\mathbf{C}^{\gamma}_{\mathbf{2v2}}$ are the following matrices.

$$\mathbf{C}^{\gamma}_{\mathbf{2i2}} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \tag{2.3.14a}$$

$$\mathbf{C}^{\gamma}_{\mathbf{2is}} = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix} \tag{2.3.14b}$$

$$\mathbf{C}^{\gamma}_{\mathbf{2v2}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \tag{2.3.14c}$$

The previous equations model the state-space representation of the LCL filter of the parallel converter in γ coordinates.

2.3.3 DC-Link model

The series and parallel converter are interconnected through the DC-Link. The DC-Link voltage is modeled as follows.

$$C_{dc}\frac{\mathrm{d}v_{dc}}{\mathrm{d}t} + \frac{1}{R_{dc}}v_{dc} = -\underbrace{(s_{1a}i_{1a} + s_{1b}i_{1b} + s_{1c}i_{1c})}_{s_1 \cdot i_1 = s_1^{\top} i_1} - \underbrace{(s_{2a}i_{2a} + s_{2b}i_{2b} + s_{2c}i_{2c})}_{s_2 \cdot i_2 = s_2^{\top} i_2} \tag{2.3.15}$$

where v_{dc} is the DC-Link voltage, s_1 and s_2 are the commutation states of the series and parallel converter, respectively. The right-side term of the previous equation can be written as the dot product of the switching state and the power converter currents. Then, multiplying both sides of the equation by the DC-Link voltage, the following is obtained.

$$C_{dc}v_{dc}\frac{\mathrm{d}v_{dc}}{\mathrm{d}t} + \frac{1}{R_{dc}}v_{dc}^2 = -v_{dc}s_1 \cdot i_1 - v_{dc}s_2 \cdot i_2 \tag{2.3.16}$$

The following equation is obtained by applying the derivative chain rule to the previous equation and considering that the multiplication between the DC-Link voltage and the switching state corresponds to the output voltage of the power converter.

$$\frac{C_{dc}}{2}\frac{\mathrm{d}v_{dc}^2}{\mathrm{d}t} + \frac{1}{R_{dc}}v_{dc}^2 = -\underbrace{v_{d2}^{\top} i_1}_{p_1} - \underbrace{v_{d2}^{\top} i_2}_{p_2} \tag{2.3.17}$$

where the terms $v_{d1}^{\top} i_1$ and $v_{d2}^{\top} i_2$ correspond to the instant active power of the series and parallel converter, respectively. Both powers can be written using the $\alpha\beta$ coordinates.

$$p_1 = \frac{3}{2}(v_{d1\alpha} i_{1\alpha} + v_{d1\beta} i_{1\beta}) \tag{2.3.18}$$

$$p_2 = \frac{3}{2}(v_{d2\alpha} i_{2\alpha} + v_{d2\beta} i_{2\beta}) \tag{2.3.19}$$

The relation between the power, the currents, and the voltages is nonlinear. Harmonics or unbalanced terms will generate oscillations in the capacitor voltage.

2.4 Combined AC model

This section shows the combined model of the series and parallel converters of the HDT. Both systems are interconnected through their inputs/output variables. In the case of the series converter, the interconnection with the parallel converter is done through the CT current, i_x. Conversely, the induced voltage v_x corresponds to the input that interconnects the parallel converter to the series converter.

2.4.1 Series converter - Coupling transformer current

The current through the primary winding of the CTs can be written in terms of the grid current as follows.

$$i_x = N_{se} i_g \tag{2.4.1}$$

Then, taking Fig. 2.4 as a reference, the dependency of the grid current with the secondary-side current, neglecting the magnetizing currents, is modeled by the following equations.

$$i_{ga} = N_{sp}(i_{sa} - i_{sc}) \tag{2.4.2a}$$
$$i_{gb} = N_{sp}(i_{sb} - i_{sa}) \tag{2.4.2b}$$
$$i_{gc} = N_{sp}(i_{sc} - i_{sa}) \tag{2.4.2c}$$

which in its matrix form is represented as follows.

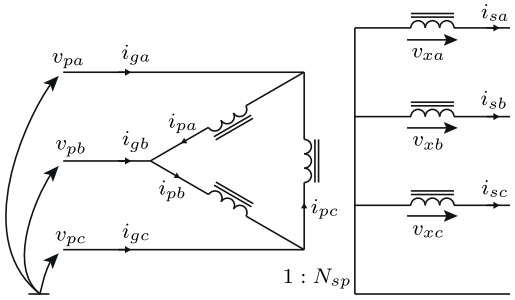


Fig. 2.4. LFT winding configuration and associated variables.

$$i_{g_{abc}} = N_{sp} \underbrace{\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}}_{\mathbf{K_T^{abc}}} i_{s_{abc}} \tag{2.4.3}$$

At the same time, the grid and secondary side currents can be written in terms of its $\alpha\beta\gamma$ components.

$$i_{g_{abc}} = \mathbf{T_{abc}} i_{g_{\alpha\beta\gamma}} \tag{2.4.4a}$$

$$i_{s_{abc}} = \mathbf{T_{abc}} i_{s_{\alpha\beta\gamma}} \tag{2.4.4b}$$

where the transformation matrix, $\mathbf{T_{abc}} = \mathbf{T}_{\alpha\beta\gamma}^{-1}$, is written as follows.

$$\mathbf{T_{abc}} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \tag{2.4.5}$$

Then, replacing (2.4.4) into (2.4.3), the following expression is obtained.

$$\mathbf{T_{abc}} i_{g_{\alpha\beta\gamma}} = N_{sp} \mathbf{K_T^{abc}} \mathbf{T_{abc}} i_{s_{\alpha\beta\gamma}} \tag{2.4.6}$$

After pre-multiplying both sides of the previous equations by $\mathbf{T}_{\alpha\beta\gamma}$, the grid current in $\alpha\beta\gamma$ coordinates is obtained.

$$i_{g_{\alpha\beta\gamma}} = N_{sp} \underbrace{\mathbf{T}_{\alpha\beta\gamma}\mathbf{K}_{\mathbf{T}}^{\mathbf{abc}}\mathbf{T}_{\mathbf{abc}}}_{\mathbf{K}_{\mathbf{T}}^{\alpha\beta\gamma}} i_{s_{\alpha\beta\gamma}} \tag{2.4.7}$$

where $\mathbf{K}_{\mathbf{T}}^{\alpha\beta\gamma}$ corresponds to the equivalent rotation matrix in $\alpha\beta\gamma$ coordinates, which is shown as follows.

$$\mathbf{K}_{\mathbf{T}}^{\alpha\beta\gamma} = \frac{\sqrt{3}}{2}\begin{bmatrix} \sqrt{3} & 1 & 0 \\ -1 & \sqrt{3} & 0 \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} \mathbf{K_T} & & 0 \\ & & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2.4.8}$$

It can be seen that the rows and columns associated with the γ component are zero, which agrees with the fact that the common mode component is removed when transferring the quantities from one side to the other of a $\Delta - Y$ transformer. Therefore, only the $\alpha\beta$ components will be taken into consideration. The grid current in $\alpha\beta$ components is given below.

$$i_{g\alpha\beta} = N_{sp}\mathbf{K_T} i_{s\alpha\beta} \tag{2.4.9}$$

Then, the primary side current of the CT, in terms of the secondary side current, is written as follows.

$$i_{x\alpha\beta} = N_{sp}N_{se}\mathbf{K_T} i_{s\alpha\beta} \tag{2.4.10}$$

Considering the previous equation and the state-space representation of (2.2.6), the final representation of the series converter with the secondary-side current as a disturbance is given below.

$$\dot{x}_{1\alpha\beta} = \mathbf{A_{c1}} x_{1\alpha\beta} + \mathbf{B_{c1}} v_{d1\alpha\beta} + \underbrace{N_{sp}N_{se}\mathbf{P_{c1}}\mathbf{K_T}}_{\mathbf{P_{c1is}}} i_{s\alpha\beta} \tag{2.4.11}$$

where $\mathbf{P_{c1is}}$ corresponds to the new input matrix that relates the secondary-side current to the series converter dynamics.

2.4.2 Parallel converter - Induced voltage

Taking Fig. 2.4 as a reference, and considering that v_p is the primary side voltage of the transformer measured with respect to a virtual neutral, the voltage induced on the secondary side is given as follows.

$$v_{xa} = N_{sp}(v_{pa} - v_{pb}) \tag{2.4.12a}$$
$$v_{xb} = N_{sp}(v_{pb} - v_{pc}) \tag{2.4.12b}$$
$$v_{xc} = N_{sp}(v_{pc} - v_{pa}) \tag{2.4.12c}$$

The previous equation written in its matrix form is given as follows.

$$v_{x_{abc}} = N_{sp} \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}}_{\mathbf{K_T^{abc\top}}} v_{p_{abc}} \tag{2.4.13}$$

Applying the same process as in the previous section, the equivalent transformation matrix in $\alpha\beta\gamma$ is obtained.

$$\mathbf{K_T^{\alpha\beta\gamma\top}} = \frac{\sqrt{3}}{2} \begin{bmatrix} \sqrt{3} & -1 & 0 \\ 1 & \sqrt{3} & 0 \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} \mathbf{K_T^\top} & & 0 \\ & & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2.4.14}$$

Taking into consideration only the $\alpha\beta$ components, due to the γ component being removed during the transformation, the induced voltage on the secondary side in terms of the primary voltage is written as follows

$$v_{x\alpha\beta} = N_{sp}\mathbf{K_T^\top} v_{p\alpha\beta} \tag{2.4.15}$$

where the primary side voltage, v_p, can be written in terms of the grid voltage, v_g, and the LC filter capacitor voltage, v_1.

$$v_{x\alpha\beta} = N_{sp}\mathbf{K_T^\top} v_{g\alpha\beta} + N_{sp}N_{se}\mathbf{K_T^\top} v_{1\alpha\beta} \tag{2.4.16}$$

Considering the previous equation and the state-space representation of (2.3.5), the equivalent model of the parallel converter is given as follows.

$$\dot{x}_{2\alpha\beta} = \mathbf{A_{c2}} x_{2\alpha\beta} + \mathbf{B_{c2}} v_{d2\alpha\beta} + \underbrace{N_{sp}\mathbf{P_{c2v}}\mathbf{K_T^\top}}_{\mathbf{P_{c2vg}}} v_{g\alpha\beta} + \underbrace{N_{sp}N_{se}\mathbf{P_{c2v}}\mathbf{K_T^\top}}_{\mathbf{P_{c2v1}}} v_{1\alpha\beta} + \mathbf{P_{c2i}} i_{L\alpha\beta} \tag{2.4.17}$$

where $\mathbf{P_{c2vg}}$ and $\mathbf{P_{c2v1}}$ are the new input matrices that relate the grid voltage and the

capacitor voltage of the LC filter to the state variables of the parallel converter.

2.4.3 Combined model

The combined model of the HDT is presented in Fig. 2.5 as a circuit model and in block diagrams in $\alpha\beta$ and γ components. As shown before, the γ component only influences the secondary side circuit, and therefore there is no interaction between the LCL and LC circuits. For the $\alpha\beta$ components, the complete model is obtained by combining both state-space representations. Equations (2.4.11) and (2.4.17) can be merged into one single model, considering $v_{g\alpha\beta}$ and $i_{L\alpha\beta}$ as the disturbances of the HDT. Then, the expanded state vector, $x_{\alpha\beta}$, and the controlled input vector, $v_{d\alpha\beta}$, are given as follows.

$$x_{\alpha\beta} = \begin{bmatrix} v_{1\alpha\beta} \\ i_{1\alpha\beta} \\ i_{2\alpha\beta} \\ i_{s\alpha\beta} \\ v_{2\alpha\beta} \end{bmatrix} \tag{2.4.18}$$

$$v_{d\alpha\beta} = \begin{bmatrix} v_{d1\alpha\beta} \\ v_{d2\alpha\beta} \end{bmatrix} \tag{2.4.19}$$

Then, the final state-space representation is shown below.

$$\dot{x}_{\alpha\beta} = \mathbf{A_c} x_{\alpha\beta} + \mathbf{B_c} v_{d\alpha\beta} + \mathbf{P_{cvg}} v_{g\alpha\beta} + \mathbf{P_{ci}} i_{L\alpha\beta} \tag{2.4.20}$$

where the $\mathbf{A_c}$, $\mathbf{B_c}$, $\mathbf{P_{cvg}}$, and $\mathbf{P_{ci}}$ matrices are presented below.

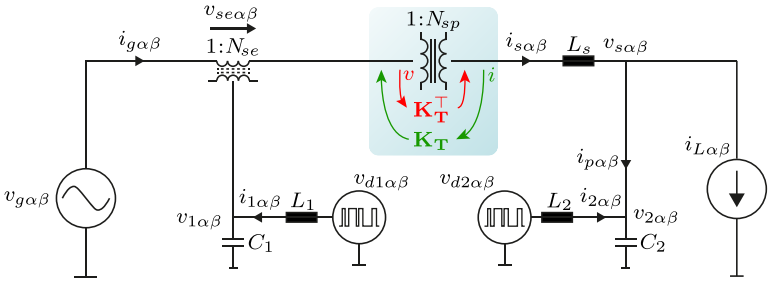
$$\mathbf{A_c} = \begin{bmatrix} \mathbf{A_{c1}} & \mathbf{P_{cis}C_{2is}} \\ \mathbf{P_{c2v1}C_{1v1}} & \mathbf{A_{c2}} \end{bmatrix} \tag{2.4.21a}$$

$$\mathbf{B_c} = \begin{bmatrix} \mathbf{B_{c1}} & \mathbf{O} \\ \mathbf{O} & \mathbf{B_{c2}} \end{bmatrix} \tag{2.4.21b}$$

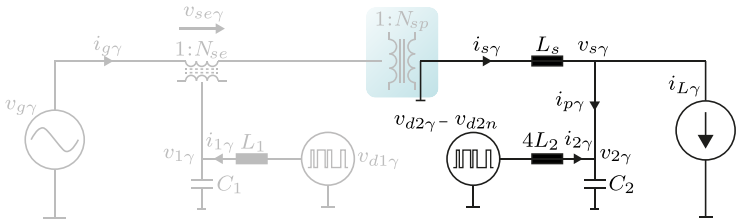
$$\mathbf{P_{cvg}} = \begin{bmatrix} \mathbf{O} \\ \mathbf{P_{c2vg}} \end{bmatrix} \tag{2.4.21c}$$

$$\mathbf{P_{ci}} = \begin{bmatrix} \mathbf{O} \\ \mathbf{P_{c2i}} \end{bmatrix} \tag{2.4.21d}$$

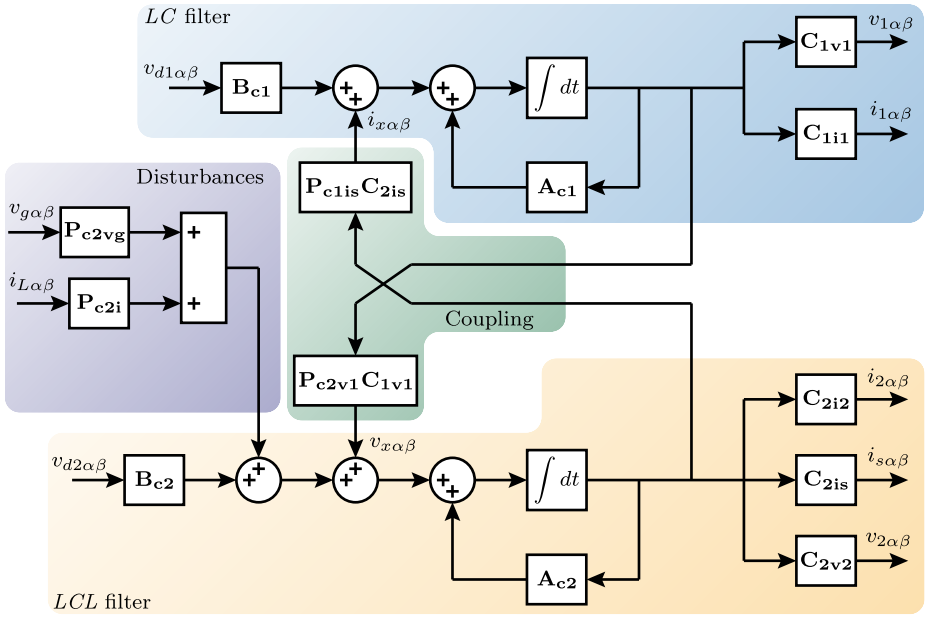
The previous state-space representation models the HDT, and it considers that both



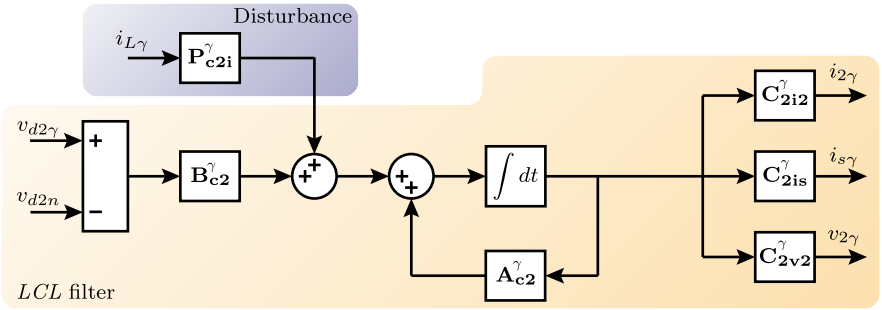
(a)



(b)



(c)



(d)

Fig. 2.5. Combined model of the HDT based on the state-space representation. **(a)** Circuit model in $\alpha\beta$ coordinates. **(b)** Circuit model in γ component. **(c)** Block diagram in $\alpha\beta$ components. **(d)** Block diagram in γ component.

power converters are interconnected only through the main transformer. The system consists of two controlled inputs, which are $v_{d1\alpha\beta}$ and $v_{d2\alpha\beta}$, and two disturbances, $v_{g\alpha\beta}$ and $i_{L\alpha\beta}$. The DC-Link model can be treated separately if $v_{d1\alpha\beta}$ and $v_{d2\alpha\beta}$ are ideal voltage sources.

2.4.4 Open-loop characteristic of the HDT

In this section, the open-loop characteristic of the HDT is presented and compared with the characteristic of its independent subsystems. For the isolated series converter, the capacitor voltage with respect to the power converter output voltage is given by the following equation.

$$v_{1\alpha\beta} = \frac{1}{L_1 C_1 s^2 + 1} v_{d1\alpha\beta} \tag{2.4.22}$$

which corresponds to a second-order system, with a resonance frequency equal to

$$\omega_{1r} = \sqrt{\frac{1}{L_1 C_1}} \tag{2.4.23}$$

For the parallel converter, the converter current with respect to the power converter output voltage is given as follows.

$$i_{2\alpha\beta} = \frac{1}{s} \frac{L_s C_2 s^2 + 1}{L_2 L_s C_2 s^2 + L_2 + L_s} v_{d2\alpha\beta} \tag{2.4.24}$$

corresponding to a third-order system with a pole in the origin. Also, the resonance frequency and the frequency at which the zero is located are given by the following equations.

$$\omega_{2r} = \sqrt{\frac{L_2 + L_s}{L_2 L_s C_2}} \tag{2.4.25a}$$

$$\omega_{2z} = \sqrt{\frac{1}{L_s C_2}} \tag{2.4.25b}$$

On the other hand, when the whole system is considered, the dynamics of both LC and LCL filters are coupled. The following equations show the complete output equations.

$$v_{1\alpha\beta} = \mathbf{C_{v1}}(s\mathbf{I} - \mathbf{A_c})^{-1}\mathbf{B_{c1}} v_{d1\alpha\beta} \tag{2.4.26a}$$

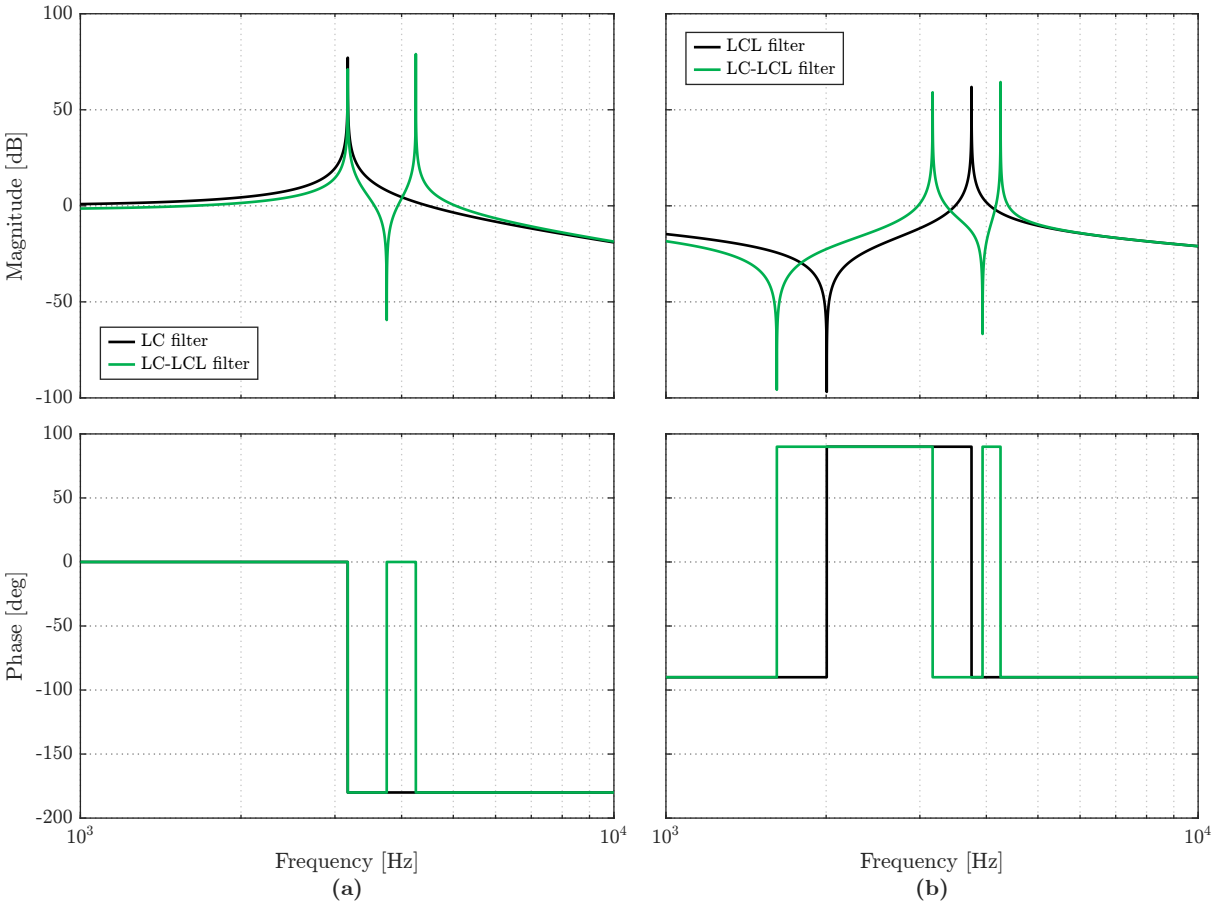


Fig. 2.6. Bode diagrams comparison. **(a)** $v_{1\alpha}/v_{d1\alpha}$. **(b)** $i_{2\alpha}/v_{d2\alpha}$.

$$v_{1\alpha\beta} = \frac{L_2L_sC_2s^2+L_2+L_s}{L_1L_2L_sC_1C_2s^4+(L_1C_1(L_2+L_s)+L_2C_2(3N_{sp}^2N_{se}^2L_1+L_s))s^2+3N_{sp}^2N_{se}^2L_1+L_2+L_s}v_{d1\alpha\beta} \tag{2.4.26b}$$

$$i_{2\alpha\beta} = \mathbf{C_{i2}}(s\mathbf{I}-\mathbf{A_c})^{-1}\mathbf{B_{c2}}v_{d2\alpha\beta} \tag{2.4.27a}$$

$$i_{2\alpha\beta} = \frac{1}{s}\frac{L_1L_sC_1C_2s^4+(L_1C_1+3N_{sp}^2N_{se}^2L_1C_2+L_sC_2)s^2+1}{L_1L_2L_sC_1C_2s^4+(L_1C_1(L_2+L_s)+L_2C_2(3N_{sp}^2N_{se}^2L_1+L_s))s^2+3N_{sp}^2N_{se}^2L_1+L_2+L_s}v_{d2\alpha\beta} \tag{2.4.27b}$$

Fig. 2.6 show the bode diagrams of the transfer functions of the LC and LCL filters against the response provided by the combined system. By simple inspection, it can be seen that the number of resonance frequencies increases, and their location is shifted. Moreover, for both transfer functions, additional zeros are present in the system. The resonance frequencies of the complete model are given by the following equation.

$$\omega_{r_{12}} = \frac{L_1C_1(L_2+L_s)+C_2L_2(L_1+L_s) \pm \mu}{2L_1L_2L_sC_1C_2} \tag{2.4.28a}$$

$$\mu = \sqrt{(L_1C_1(L_2+L_s)+C_2L_2(L_1+L_s))^2 - 4L_1L_2C_1C_2(L_1+L_2+L_s)} \tag{2.4.28b}$$

Then, in the case of the capacitor voltage transfer function, a zero is present in the following frequency.

$$\omega_{zv} = \sqrt{\frac{L_2+L_s}{L_2L_sC_2}} = \omega_{2r} \tag{2.4.29}$$

which corresponds to the resonance frequency of the LCL filter. On the other side, the frequencies at which the zeros occur in the converter current response are written as follows.

$$\omega_{zv_{12}} = \frac{(L_1C_1+L_1C_2+L_sC_2) \pm \sqrt{(L_1C_1+L_1C_2+L_sC_2)^2 - 4L_1L_sC_1C_2}}{2L_1L_sC_1C_2} \tag{2.4.30}$$

It is known that the effect of the resonance frequencies of LC and LCL affect the performance of power converters, which can trigger instabilities can be triggered. Therefore, for the proposed HDT, a robust controller must be employed to guarantee a stable operation.

2.5 Discrete dq model

In the literature, it can be found the discrete-time dq frame modeling of power converters is done using the continuous-time dq frame representation of the system, as shown in Fig. 2.7(a). This is an incorrect assumption because the Zero order Hold (ZOH) is being applied to the converter output voltage, which is then modulated, in the abc frame using a discrete rotation angle. Therefore, this section summarizes the discrete-time dq model of the HDT based on the model written in $\alpha\beta$ coordinates.

Taking as a reference the continuous-time combined model of the HDT of (2.4.20), its discrete state-space representation in $\alpha\beta$ coordinates is given as follows.

$$x_{\alpha\beta}[k+1] = \mathbf{\Phi}_{\alpha\beta}x_{\alpha\beta}[k] + \mathbf{\Psi}_{\alpha\beta}\mathbf{B_c}v_{d\alpha\beta}[k] + \mathbf{\Psi}_{\alpha\beta}\mathbf{P_{cvg}}v_{g\alpha\beta}[k] + \mathbf{\Psi}_{\alpha\beta}\mathbf{P_{ci}}i_{L\alpha\beta}[k] \tag{2.5.1}$$

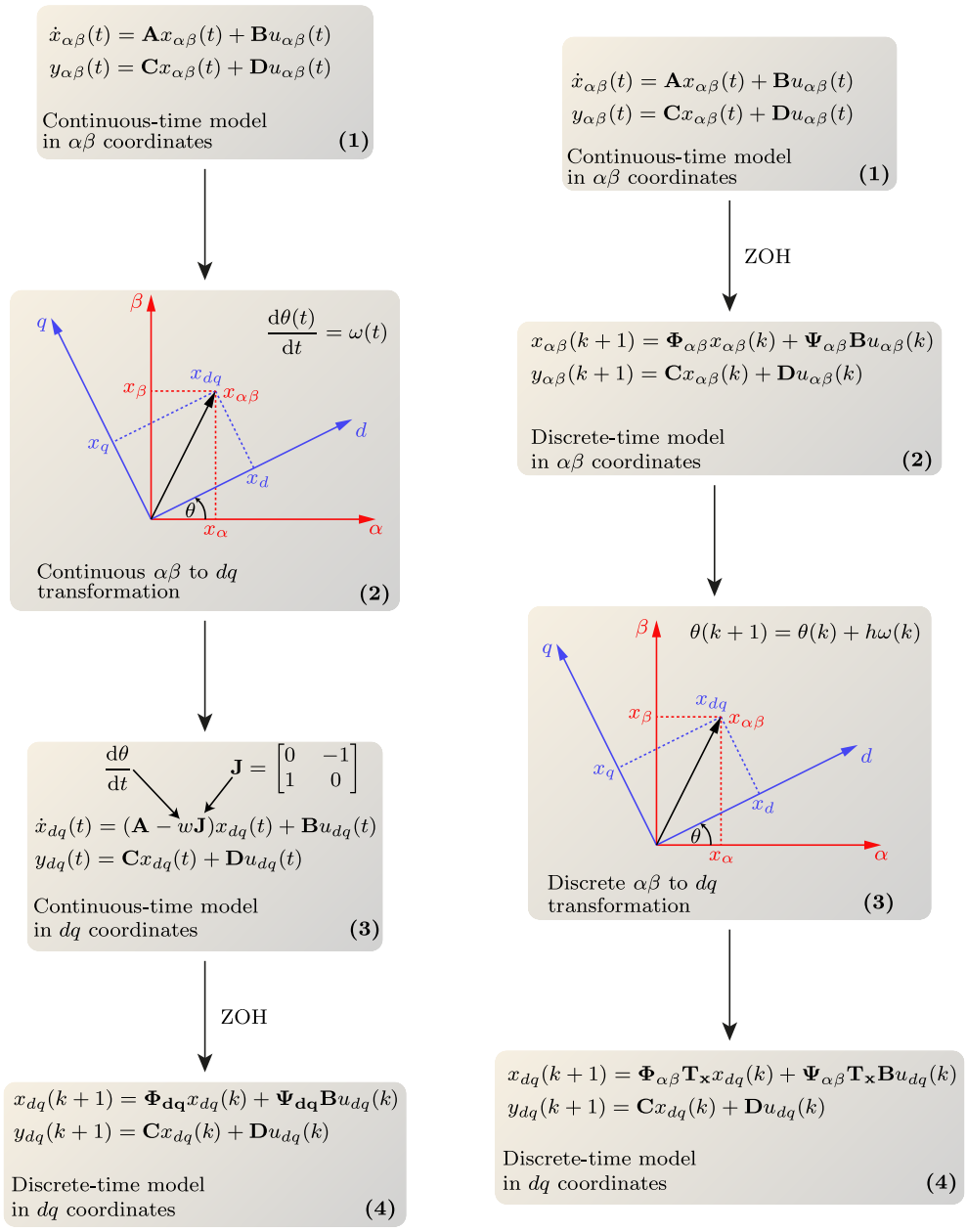


Fig. 2.7. Discrete-time $\alpha\beta$ to dq transformation. **(a)** Incorrect procedure. **(b)** Correct procedure.

where $\mathbf{\Phi}_{\alpha\beta}$ and $\mathbf{\Psi}_{\alpha\beta}$ are given as follows when using the ZOH transformation with a sample time equal to h.

$$\mathbf{\Phi}_{\alpha\beta} = e^{\mathbf{A_c}h} \tag{2.5.2a}$$

$$\mathbf{\Psi}_{\alpha\beta} = \int_0^h e^{\mathbf{A_c}s} ds \tag{2.5.2b}$$

The discrete-time model in the dq reference frame is obtained based on the solution in $\alpha\beta$ coordinates, as follows.

$$x_{dq}[k+1] = \mathbf{\Phi}_{\alpha\beta}\mathbf{T_x}x_{dq}[k'] + \mathbf{\Psi}_{\alpha\beta}\mathbf{T_x}\mathbf{B_c}v_{ddq}[k] + \mathbf{\Psi}_{\alpha\beta}\mathbf{T_x}\mathbf{P_{cvg}}v_{gdq}[k] + \mathbf{\Psi}_{\alpha\beta}\mathbf{T_x}\mathbf{P_{ci}}i_{Ldq}[k] \tag{2.5.3}$$

where $\mathbf{T_x}$ corresponds to a diagonal block matrix containing the rotation matrix $\mathbf{T}$.

$$\mathbf{T_x} = \begin{bmatrix} \mathbf{T} & 0 & \cdots & 0 \\ 0 & \mathbf{T} & & 0 \\ \vdots & & \ddots & 0 \\ 0 & 0 & & \mathbf{T} \end{bmatrix}_{2nx2n} \tag{2.5.4a}$$

$$\mathbf{T} = \begin{bmatrix} \cos(\omega h) & \sin(\omega h) \\ -\sin(\omega h) & \cos(\omega h) \end{bmatrix} \tag{2.5.4b}$$

Therefore, the transformation from the discrete system in $\alpha\beta$ coordinates to the dq frame is a straightforward procedure, only requiring the postmultiplication of $\Phi_{\alpha\beta}$ and $\Psi_{\alpha\beta}$ by the transformation block matrix $\mathbf{T_x}$. The latter is equivalent to a phase shift of $-\omega h$. The correct transformation procedure is summarized in Fig. 2.7(b).

2.6 Conclusion

This chapter presented the diagram of the proposed HDT configuration, which is composed of a series converter connected to the MV side and a parallel converter connected to the LV side. The continuous-time state-space representation of each of the stages of the HDT and the combined model were presented. Finally, the frequency characteristic of the HDT was introduced, comparing it with its individual converter counterpart. Due to the interaction of the LC and LCL filter, additional resonances are observed.

The previous models will be used during the rest of this thesis for simulation, analysis, and control design purposes.

Chapter 3

BALANCED OPERATION AND STABILITY OF THE HDT

Remark: This chapter is partly based on the following publication of the author:

[1] A. Carreno, M. Malinowski, and M. A. Perez, "Stability Analysis of a Hybrid Distribution Transformer with a Series/Parallel Converter Connected to the Primary/Secondary Side", *2024 4th International Conference on Smart Grid and Renewable Energy (SGRE)*, Doha, Qatar, 2024, pp. 1-6.

This chapter presents the control system of the HDT in the *dq* reference frame when operating under balanced conditions. Then, the stability of the HDT is assessed, for which the interaction of the AC circuit and internal controllers is taken into consideration. The stability of HDT is analyzed using the equivalent impedance/admittance models.

The parallel and series converters are coupled through the main LFT, and also through the DC-Link. Nonetheless, in order to simplify the evaluation, the DC coupling will be neglected, as well as the dynamics associated with the PLLs and external controllers.

Therefore, only the internal stability will be assessed considering the AC circuit, assuming that each power converter is supplied by ideal DC sources.

Once the controllers are obtained, the impedance and admittance models of the series and parallel converters are obtained. To interconnect the impedance and admittance models of each converter, the approximate continuous-time models are employed. Therefore, the computation delay and the PWM delay are approximated as follows.

$$\mathbf{G_{del}} = \begin{bmatrix} e^{-1.5hs} & 0 \\ 0 & e^{-1.5hs} \end{bmatrix} \tag{3.0.1}$$

Because the model is done in the dq reference frame, which results in coupled transfer functions, the SISO stability analysis tools can not be utilized. Then, MIMO stability analysis tools must be employed, such as the Generalized Nyquist Criterion (GNC), and also the use of singular values.

3.1 Control system in dq coordinates

The diagram shown in Fig. 3.1 summarizes the control algorithm of the HDT in the dq reference frame. This diagram contains the internal current and voltage controllers, as well as the external DC-Link voltage controller and grid voltage compensator.

Remark: The controller gains are designed using the Linear Quadratic Regulator (LQR), for which the converter dynamics and controller must be represented in the state-space form. To avoid repetition, the step-by-step process is presented in **Chapter 5** in a much broader context. Additionally, in **Appendix A** the LQR background is provided for continuous and discrete-time systems.

3.1.1 Series converter

As Fig. 3.1(a) shows, the internal controller regulates the capacitor voltage, v_1. The controller and the damping term associated with the converter current are given below.

$$\mathbf{H_{v1}} = \mathbf{K_{v1p}} + \mathbf{K_{v1i}}\frac{1}{s} \tag{3.1.1a}$$

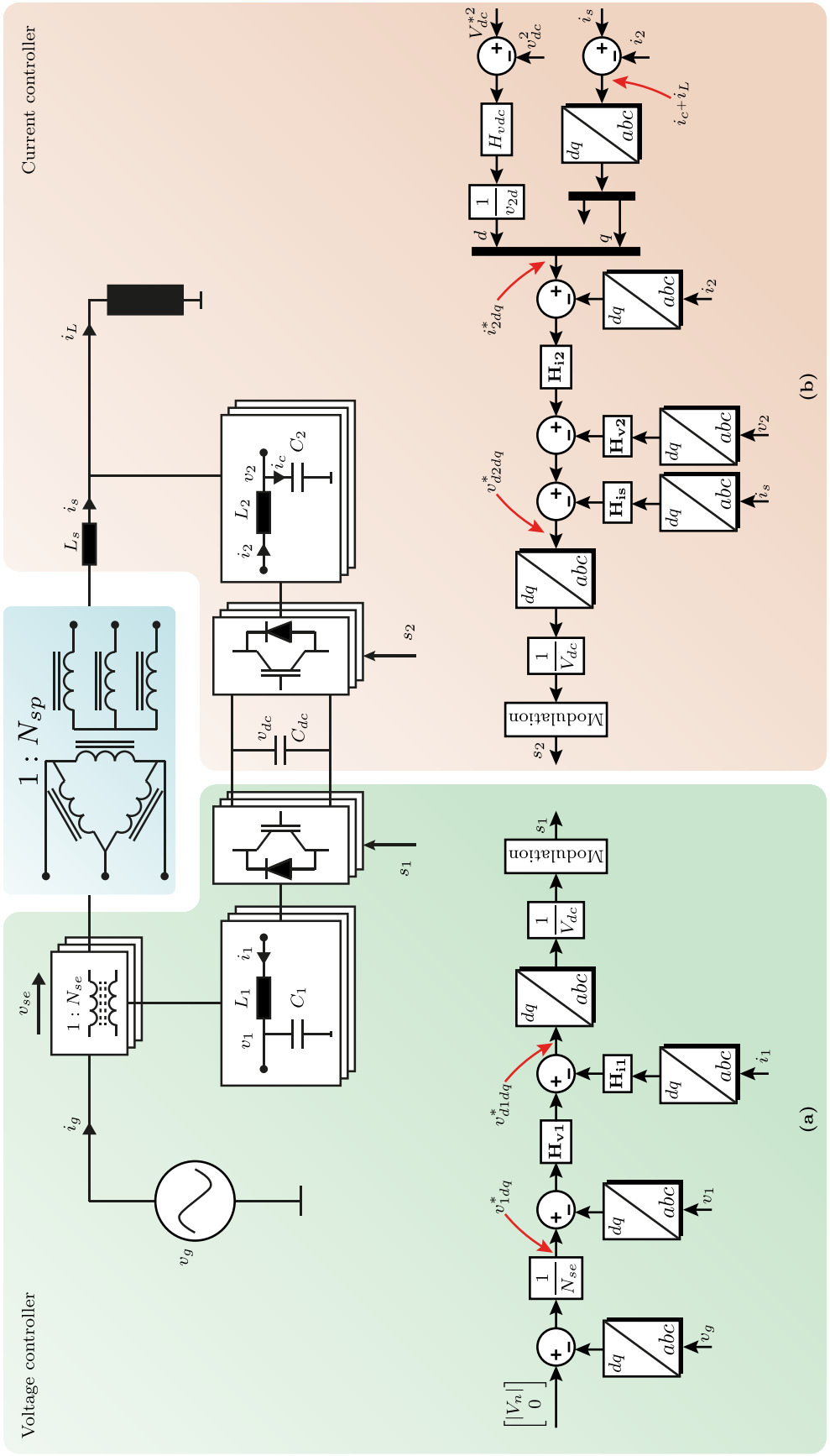


Fig. 3.1. HDT controller for balanced operation. **(a)** Voltage controller. **(b)** Current controller.

$$\mathbf{H_{i1}} = \mathbf{K_{i1p}} \tag{3.1.1b}$$

The series controller is synchronized to the phase angle of the grid voltage, therefore the capacitor voltage reference corresponds to the deviation of the grid voltage from its nominal value. It is obtained as follows.

$$v^*_{1dq} = \frac{1}{N_{se}} \left(\begin{bmatrix} |V_n| \\ 0 \end{bmatrix} - v_{gdq} \right) \tag{3.1.2}$$

In this chapter, it will be assumed that all the measurements required by the series controller are employed, i.e., the grid voltage, capacitor voltage, and power converter current measurements are available.

3.1.2 Parallel converter

As Fig. 3.1(b) shows, the internal controller regulates the power converter output current, i_2. The current controller, $\mathbf{G_{i2}}$, and the damping terms associated with the secondary-side current and capacitor voltage are given as follows.

$$\mathbf{H_{i2}} = \mathbf{K_{i2p}} + \mathbf{K_{i2i}} \frac{1}{s} \tag{3.1.3a}$$

$$\mathbf{H_{is}} = \mathbf{K_{isp}} \tag{3.1.3b}$$

$$\mathbf{H_{v2}} = \mathbf{K_{v2p}} \tag{3.1.3c}$$

The parallel converter controller is synchronized to the phase angle of the secondary-side voltage, v_2. Therefore the d component, or active component, is related to the DC-Link voltage controller, which is given below.

$$H_{vdc}(s) = \frac{K_{vdcp} s + K_{vdci}}{s} \tag{3.1.4}$$

On the other side, the q component, or reactive component, corresponds to the reactive components of the load and capacitor current.

In this chapter, it will be assumed that all the measurements required by the parallel controller are employed, i.e., the secondary-side current, converter current, load current, and capacitor voltage measurements are available.

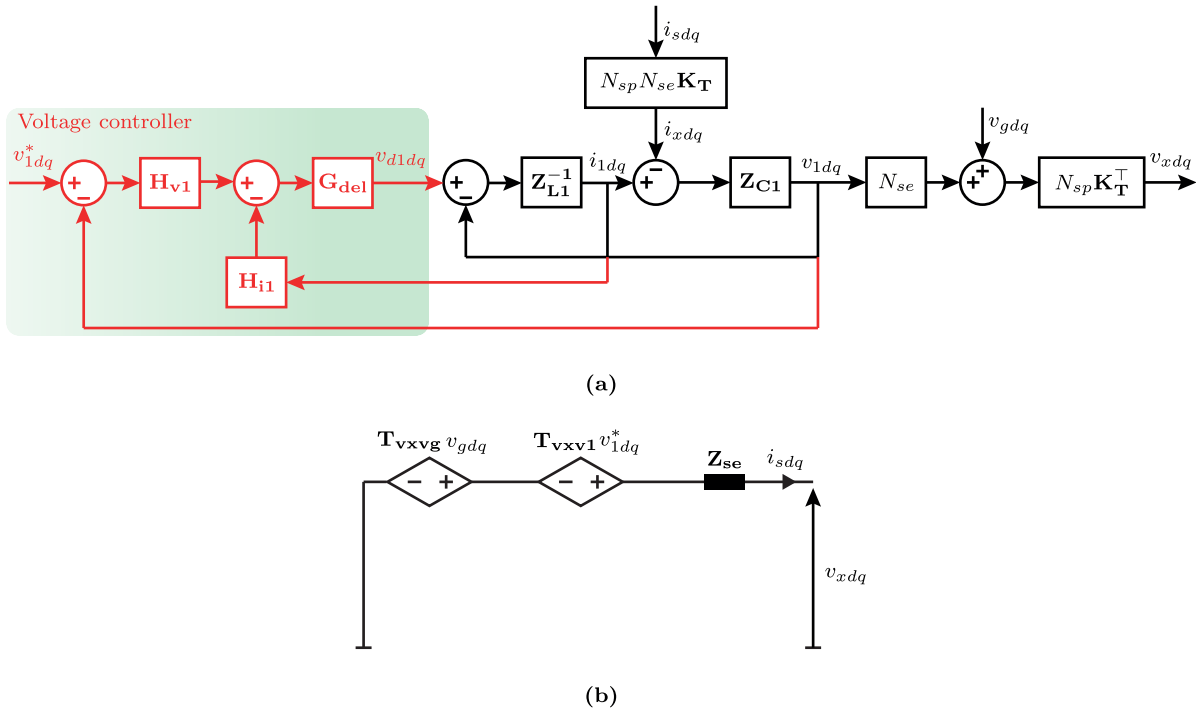


Fig. 3.2. Series converter model. **(a)** Block diagram. **(b)** Equivalent impedance model.

3.2 Series converter impedance model

The block diagram of the series converter and its controller based on the transfer function blocks is shown in Fig. 3.2(a). The output delay, $\mathbf{G_{del}}$ is included in the power converter output voltage. The filter impedances, in the *dq* frame, are defined as follows.

$$\mathbf{Z_{L1}} = \begin{bmatrix} L_1 s + R_1 & -\omega L_1 \\ \omega L_1 & L_1 s + R_1 \end{bmatrix} \tag{3.2.1a}$$

$$\mathbf{Z_{c1}}^{-1} = \begin{bmatrix} C_1 s + R_{c1} & -\omega C_1 \\ \omega C_1 & C_1 s + R_{c1} \end{bmatrix} \tag{3.2.1b}$$

The states of the system, filter voltage and power converter current, are given by the following equation.

$$x_{1dq} = \begin{bmatrix} v_{1dq} \\ i_{1dq} \end{bmatrix} = \mathbf{G_{x1vd1}} v_{d1dq} + \mathbf{G_{x1is}} i_{sdq} \tag{3.2.2}$$

where $\mathbf{G_{x1vd1}}$ and $\mathbf{G_{x1is}}$ are the transfer function matrices that relate the states of the

LC filter to the power converter output voltage and secondary side current. They are defined as follows.

$$\mathbf{G_{x1vd1}} = \begin{bmatrix} \mathbf{I} & -\mathbf{Z_{c1}} \\ {\mathbf{Z_{L1}}}^{-1} & \mathbf{I} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{O} \\ {\mathbf{Z_{L1}}}^{-1} \end{bmatrix} \tag{3.2.3a}$$

$$\mathbf{G_{x1is}} = \begin{bmatrix} \mathbf{I} & -\mathbf{Z_{c1}} \\ {\mathbf{Z_{L1}}}^{-1} & \mathbf{I} \end{bmatrix}^{-1} \begin{bmatrix} -\mathbf{Z_{c1}} \\ \mathbf{O} \end{bmatrix} \tag{3.2.3b}$$

The previous equations model the series converter in an open loop. Then, the power converter output voltage can be written as follows.

$$v_{d1dq} = \mathbf{G_{del}}\mathbf{H_{v1}}v^*_{1dq} - \mathbf{G_{del}}\mathbf{H_1}x_{1dq} \tag{3.2.4}$$

where the controller matrix $\mathbf{H_1}$ is given as follows.

$$\mathbf{H_1} = [\mathbf{H_{v1}} \quad \mathbf{H_{i1}}] \tag{3.2.5}$$

Once the control loop is closed, the filter states are obtained.

$$x_{1dq} = \mathbf{F_1}\mathbf{G_{x1vd1}}\mathbf{G_{del}}\mathbf{G_{v1}}v^*_{1dq} + \mathbf{F_1}\mathbf{G_{x1is}}i_{sdq} \tag{3.2.6}$$

where $\mathbf{F_1}$ and the the return ratio, $\mathbf{L_1}$, are given below.

$$\mathbf{F_1} = (\mathbf{I} + \mathbf{L_1})^{-1} \tag{3.2.7a}$$

$$\mathbf{L_1} = \mathbf{G_{x1vd1}}\mathbf{G_{del}}\mathbf{H_1} \tag{3.2.7b}$$

In order to obtain the equivalent impedance model of the series converter, the induced voltage of the secondary side is obtained based on the blocks diagram of Fig. 3.2(a), which is written as follows.

$$v_{xdq} = \mathbf{T_{vxv1}}v^*_{1dq} + \mathbf{Z_{se}}i_{sdq} + \mathbf{T_{vxvg}}v_{gdq} \tag{3.2.8}$$

The previous transfer function is represented in the equivalent impedance model of Fig. 3.2(b). It can be seen that the transfer function that relates the secondary current to the induced voltage on the secondary side corresponds to the equivalent series impedance of the HDT. The transfer functions are defined below.

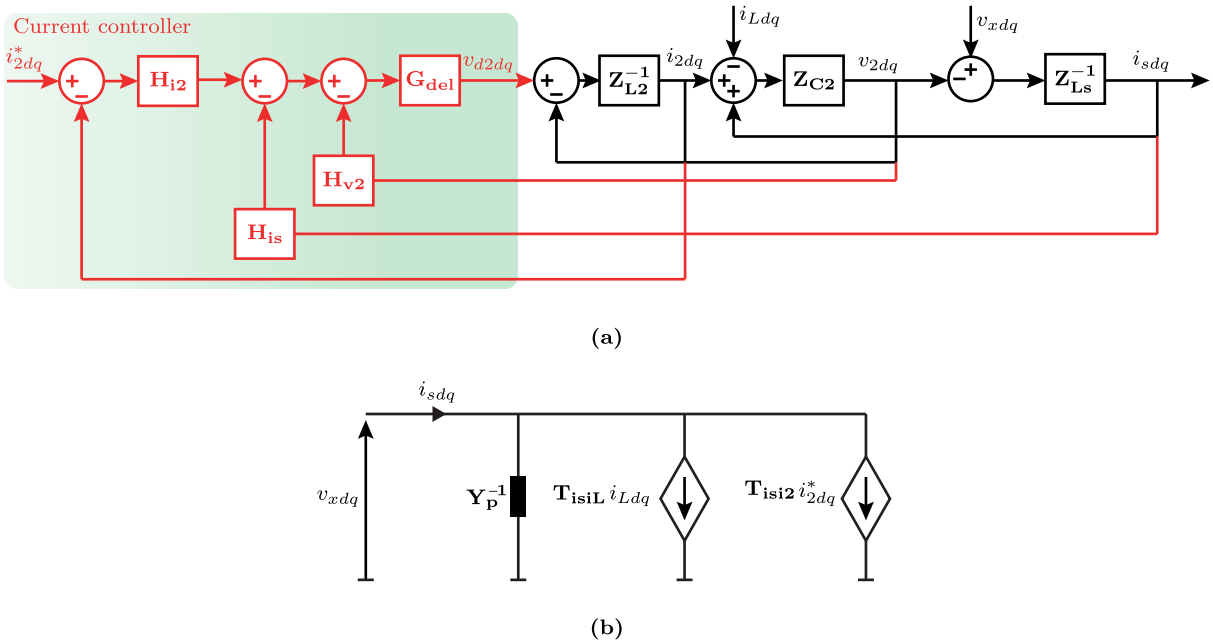


Fig. 3.3. Parallel converter model. **(a)** Block diagram. **(b)** Equivalent admittance model.

$$\mathbf{T_{vxv1}} = \mathbf{C_{1vx}F_1G_{x1vd1}G_{del}H_{v1}} \tag{3.2.9a}$$

$$\mathbf{Z_{se}} = \mathbf{C_{1vx}F_1G_{x1is}} \tag{3.2.9b}$$

$$\mathbf{T_{vxvg}} = N_{sp}\mathbf{K_T} \tag{3.2.9c}$$

where $\mathbf{C_{1vx}}$ relates the states of the LC filter to the induced secondary voltage, and it is given as follows.

$$\mathbf{C_{1vx}} = \begin{bmatrix} N_{sp}N_{se}\mathbf{K_T} & \mathbf{O} \end{bmatrix} \tag{3.2.10}$$

3.3 Parallel converter admittance model

The transfer function block model of the parallel converter and its controller are shown in Fig. 3.3(a). The system matrix impedances in the dq frame are defined below.

$$\mathbf{Z_{L2}} = \begin{bmatrix} L_2 s + R_2 & -\omega L_2 \\ \omega L_2 & L_2 s + R_2 \end{bmatrix} \tag{3.3.1a}$$

$$\mathbf{Z_{Ls}} = \begin{bmatrix} L_s s + R_s & -\omega L_s \\ \omega L_s & L_s s + R_s \end{bmatrix} \tag{3.3.1b}$$

$$\mathbf{Z_{c2}}^{-1} = \begin{bmatrix} C_2 s + R_{c2} & -\omega C_2 \\ \omega C_2 & C_2 s + R_{c2} \end{bmatrix} \tag{3.3.1c}$$

The system states, which are the power converter current, the secondary side current, and the capacitor voltage are written as follows.

$$x_{2dq} = \begin{bmatrix} i_{2dq} \\ i_{sdq} \\ v_{2dq} \end{bmatrix} = \mathbf{G_{x2vd2}} v_{d2dq} + \mathbf{G_{x2vx}} v_{xdq} + \mathbf{G_{x2iL}} i_{Ldq} \tag{3.3.2}$$

where $\mathbf{G_{x2vd2}}$, $\mathbf{G_{x2vx}}$ and $\mathbf{G_{x2iL}}$ are the transfer function matrices that relate the states of the *LCL* filter to the power converter output voltage, secondary side induce voltage, and load current, which are defined as follows.

$$\mathbf{G_{x2vd2}} = \begin{bmatrix} \mathbf{I} & \mathbf{I} & \mathbf{Z_{L2}} \\ \mathbf{O} & \mathbf{I} & \mathbf{Z_{Ls}} \\ -\mathbf{Z_{c2}} & -\mathbf{Z_{c2}} & \mathbf{O} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{Z_{L2}}^{-1} \\ \mathbf{O} \\ \mathbf{O} \end{bmatrix} \tag{3.3.3a}$$

$$\mathbf{G_{x2vx}} = \begin{bmatrix} \mathbf{I} & \mathbf{I} & \mathbf{Z_{L2}} \\ \mathbf{O} & \mathbf{I} & \mathbf{Z_{Ls}} \\ -\mathbf{Z_{c2}} & -\mathbf{Z_{c2}} & \mathbf{O} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{O} \\ \mathbf{Z_{Ls}}^{-1} \\ \mathbf{O} \end{bmatrix} \tag{3.3.3b}$$

$$\mathbf{G_{x2iL}} = \begin{bmatrix} \mathbf{I} & \mathbf{I} & \mathbf{Z_{L2}} \\ \mathbf{O} & \mathbf{I} & \mathbf{Z_{Ls}} \\ -\mathbf{Z_{c2}} & -\mathbf{Z_{c2}} & \mathbf{O} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{O} \\ \mathbf{O} \\ \mathbf{Z_{c2}} \end{bmatrix} \tag{3.3.3c}$$

Then, considering the controller matrices, the output voltage of the converter is given below.

$$v_{d2dq} = \mathbf{G_{del}} \mathbf{H_{i2}} i^*_{2dq} - \mathbf{G_{del}} \mathbf{H_2} x_{2dq} \tag{3.3.4}$$

where the controller matrix $\mathbf{H_2}$ is given as follows.

$$\mathbf{H_2} = [\mathbf{H_{i2}} \quad \mathbf{H_{is}} \quad \mathbf{H_{v2}}] \tag{3.3.5}$$

Once the control loop is closed, the filter states can be written as follows.

$$x_{2dq} = \mathbf{F_2 G_{x2vd2} G_{del} G_{i2}} i^*_{2dq} + \mathbf{F_2 G_{x2vx}} v_{xdq} + \mathbf{F_2 G_{x2iL}} i_{Ldq} \tag{3.3.6}$$

where $\mathbf{F_2}$ and the return ratio, $\mathbf{L_2}$,are written as follows..

$$\mathbf{F_2} = (\mathbf{I} + \mathbf{L_2})^{-1} \tag{3.3.7a}$$

$$\mathbf{L_2} = \mathbf{G_{x2\_vd2} G_{del} H_2} \tag{3.3.7b}$$

In order to obtain the equivalent admittance model of the parallel converter, the secondary-side current must be written in terms of the independent variables. Based on the blocks diagram of Fig. 3.3(a), the secondary side current is given as follows.

$$i_{sdq} = \mathbf{T_{isi2}} i^*_{2dq} + \mathbf{Y_p} v_{xdq} + \mathbf{T_{isiL}} i_{Ldq} \tag{3.3.8}$$

The previous transfer function is represented in the equivalent impedance model of Fig. 3.3(b). It can be seen that the transfer function that relates the secondary current to the induced voltage on the secondary side corresponds to the equivalent parallel admittance of the HDT. The transfer functions are defined below.

$$\mathbf{T_{isi2}} = \mathbf{C_{is} F_2 G_{x2vd2} G_{del} H_{i2}} \tag{3.3.9a}$$

$$\mathbf{Y_p} = \mathbf{C_{is} F_2 G_{x2vx}} \tag{3.3.9b}$$

$$\mathbf{T_{isiL}} = \mathbf{C_{is} F_2 G_{x2iL}} \tag{3.3.9c}$$

3.4 HDT combined stability

The combined circuit is shown in Fig. 3.4(a), in which the DC-Link is decoupled, and each converter is supplied by independent ideal voltage sources. Then, taking the equivalent impedance model of Fig. 3.2(b) and the equivalent admittance model of Fig. 3.3(b), the combined model of Fig. 3.4(b) is obtained.

Taking the equations of the secondary side voltage and current, and combining them into a single matrix representation, the following is obtained.

$$\begin{bmatrix} v_{xdq} \\ i_{sdq} \end{bmatrix} = \mathbf{F_{ZY}} \begin{bmatrix} \mathbf{T_{vxv1}} & \mathbf{O} \\ \mathbf{O} & \mathbf{T_{isi2}} \end{bmatrix} \begin{bmatrix} v^*_{1dq} \\ i^*_{2dq} \end{bmatrix} + \mathbf{F_{ZY}} \begin{bmatrix} \mathbf{T_{vxvg}} & \mathbf{O} \\ \mathbf{O} & \mathbf{T_{isiL}} \end{bmatrix} \begin{bmatrix} v_{gdq} \\ i_{Ldq} \end{bmatrix} \tag{3.4.1}$$

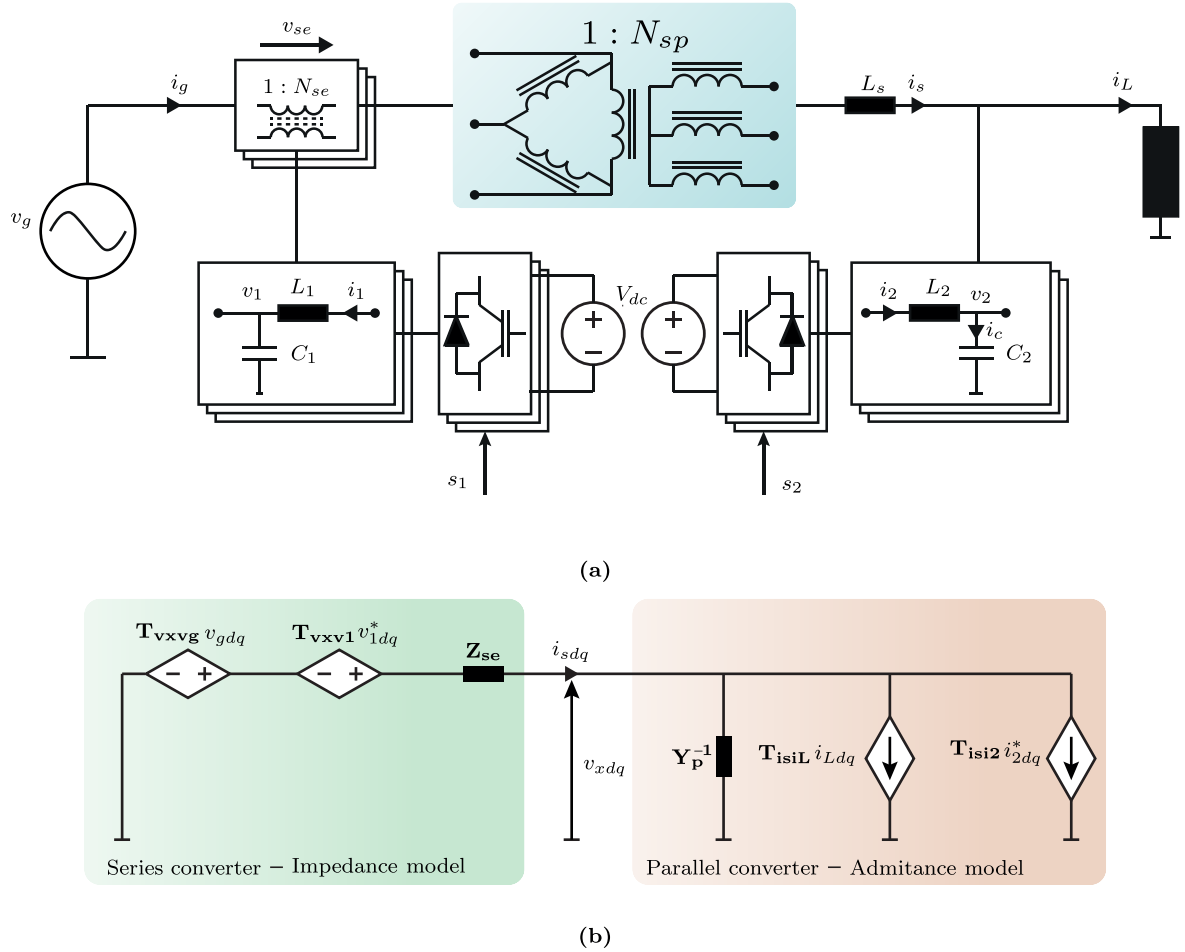


Fig. 3.4. Combined model. **(a)** Coupled AC reference model. **(b)** Combined impedance/admittance model.

where $\mathbf{F_{ZY}}$ is given below.

$$\mathbf{F_{ZY}} = \left(\begin{bmatrix} \mathbf{I} & \mathbf{O} \\ \mathbf{O} & \mathbf{I} \end{bmatrix} - \begin{bmatrix} \mathbf{O} & \mathbf{Z_{se}} \\ \mathbf{Y_p} & \mathbf{O} \end{bmatrix} \right)^{-1} \tag{3.4.2}$$

The previous equation can be written as follows.

$$\mathbf{F_{ZY}} = \begin{bmatrix} (\mathbf{I} - \mathbf{Z_{se}}\mathbf{Y_p})^{-1} & \mathbf{O} \\ \mathbf{O} & (\mathbf{I} - \mathbf{Y_p}\mathbf{Z_{se}})^{-1} \end{bmatrix} \begin{bmatrix} \mathbf{I} & \mathbf{Z_{se}} \\ \mathbf{Y_p} & \mathbf{I} \end{bmatrix} \tag{3.4.3}$$

Therefore, the stability of the HDT can be assessed based on the interaction between the equivalent series impedance and parallel admittance of each converter. The return ratio $\mathbf{L_{sep}} = -\mathbf{Z_{se}}\mathbf{Y_p}$ must comply with the GNC in order to obtain a stable system, once the series and parallel converter are interconnected.

Table 3.1. HDT parameters for balanced conditions.

HDT parameters					
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**
$\|v_g\|$	100V	$\|v_s\|$	100V	ω	$2\pi 50$
V_{dc}	250V	C_{dc}	6400μF	L_s	500μH
C_1 C_2	12.6μF	L_1 L_2	200μH	N_{se}	1/5

A robust criteria for the impedance-admittance product, is given by their maximum singular values.

$$\overline{\sigma}(\mathbf{L_{sep}}) \leq \overline{\sigma}(\mathbf{Z_{se}})\overline{\sigma}(\mathbf{Y_p}) \leq 1 \tag{3.4.4}$$

Therefore, if the product of the maximum singular values of the impedance/admittance is less than 1 for all frequencies, the coupled system will be stable, independently of the phase of its components. Alternatively, if the inverse of the series impedance is considered, the following can be stated.

$$\overline{\sigma}(\mathbf{L_{sep}}) \leq \frac{\overline{\sigma}(\mathbf{Y_p})}{\underline{\sigma}(\mathbf{Z_{se}}^{-1})} \leq 1 \tag{3.4.5}$$

Then, if the minimum singular values of the inverse of the series impedance are bigger than the maximum singular values of the admittance, and they never cross, the magnitude of the return ratio will be less than 1, and the closed-loop system will be stable.

3.5 Stability assessment

This section assesses the internal stability of the HDT considering the AC interaction of both power converters. The HDT parameters are presented in Table 3.1.

3.5.1 Series converter

To assess the internal stability of the series converter, the return ratio, $\mathbf{L_1}$, must comply with the GNC. The control parameters in Table 3.2 were obtained using the LQR. The results of plotting the eigenvalues loci are presented in Fig. 3.5(a) when the delay of the power converter is neglected, whereas the result shown in Fig. 3.5(b) takes the delay into consideration.

For the controller design, the reference model does not include the internal delays. Then, utilizing the LQR method to design the state feedback controller results in a

Table 3.2. Series converter - control parameters

Parameter	Value
$\mathbf{K_{v1p}}$	$\begin{bmatrix} 0.0539 & -0.0002 \\ 0.0002 & 0.0539 \end{bmatrix}$
$\mathbf{K_{v1i}}$	$\begin{bmatrix} 316.2234 & -1.666 \\ 1.666 & 316.2234 \end{bmatrix}$
$\mathbf{K_{i1p}}$	$\begin{bmatrix} 1.3507 & 0 \\ 0 & 1.3507 \end{bmatrix}$

Table 3.3. Parallel converter - control parameters

Parameter	Value
$\mathbf{K_{i2p}}$	$\begin{bmatrix} 1.2923 & 0 \\ 0 & 1.2923 \end{bmatrix}$
$\mathbf{K_{i2i}}$	$\begin{bmatrix} 302.2395 & -93.0124 \\ 93.0124 & 302.2395 \end{bmatrix}$
$\mathbf{K_{isp}}$	$\begin{bmatrix} 0.5526 & 0.0004 \\ -0.0004 & 0.5526 \end{bmatrix}$
$\mathbf{K_{v2p}}$	$\begin{bmatrix} 0.0453 & 0.0008 \\ -0.0008 & 0.0453 \end{bmatrix}$

system with high phase and gain margins. For the specific controller, the gain margin is infinite, and the phase margin is equal to 95°. As expected, once the delays are taken into consideration, the stability margins are reduced. In this specific case, the phase margin is reduced to 72.4°, whereas the gain margin is equal to 4, which corresponds to robust stability margins.

As the return ratio $\mathbf{L_1}$ complies with the GNC, the internal stability of the series converter is assured. Then, the equivalent series impedance and the transfer functions that model the induced secondary side voltage are also stable.

3.5.2 Parallel converter

The internal stability of the parallel converter is evaluated in a similar manner as in the series converter, i.e., studying the return ratio and checking if it complies with the GNC. The results of plotting the eigenvalues loci are presented in Fig. 3.6(a) when the delay of the power converter are neglected, whereas the results shown in Fig. 3.6(b) takes the delay

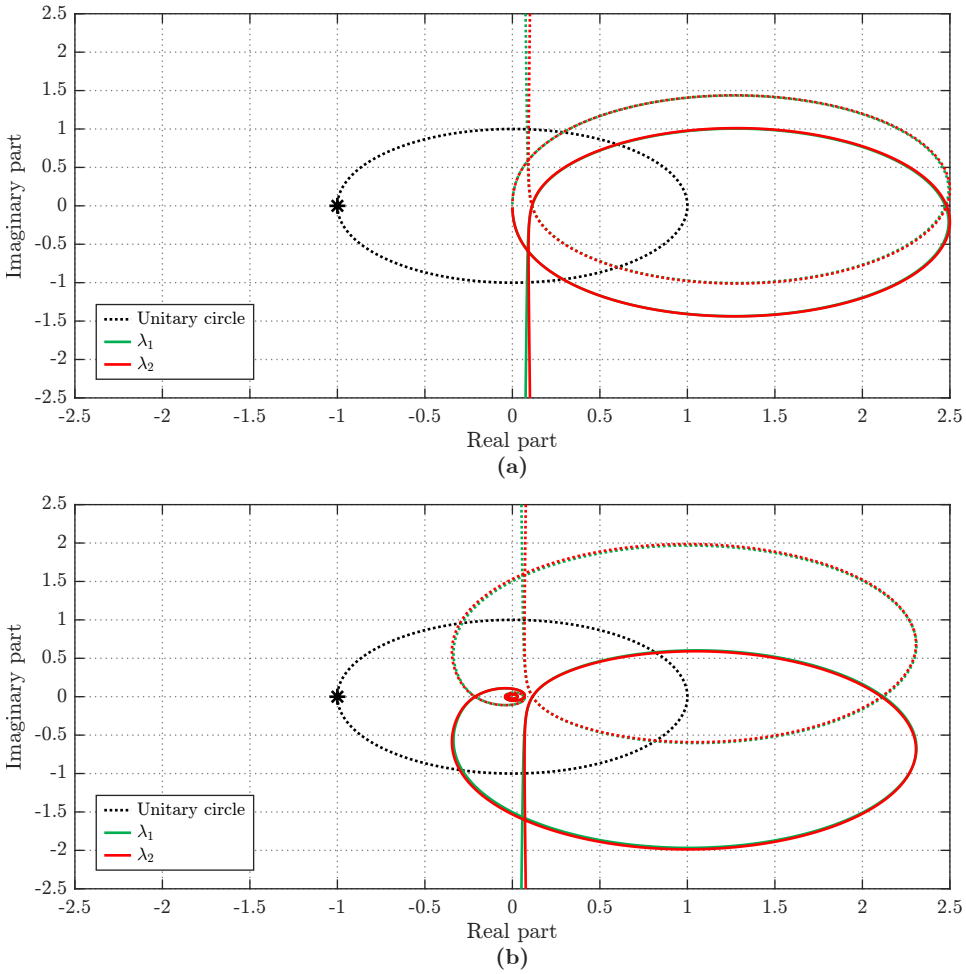


Fig. 3.5. Series converter - Nyquist plot of the eigenvalues of the capacitor voltage control open loop. **(a)** No delay. **(b)** With delay.

into consideration. For this, the controller parameters shown in Table 3.3 were obtained using the LQR.

As for the series converter, the reference model does not include the internal delays. Then, utilizing the LQR method to design the state feedback controller results in a system with high phase and gain margins. For the specific controller, the gain margin is infinite, and the phase margin is equal to 85°. As expected, once the delays are taken into consideration, the stability margin is reduced. In this specific case, the phase margin is reduced to 82.6°, whereas the gain margin is equal to 4, which corresponds to robust stability margins.

As the return ratio $\mathbf{L_2}$ complies with the GNC, the internal stability of the parallel converter is assured. Then, equivalent parallel admittance and the transfer functions that model the secondary side current are also stable.

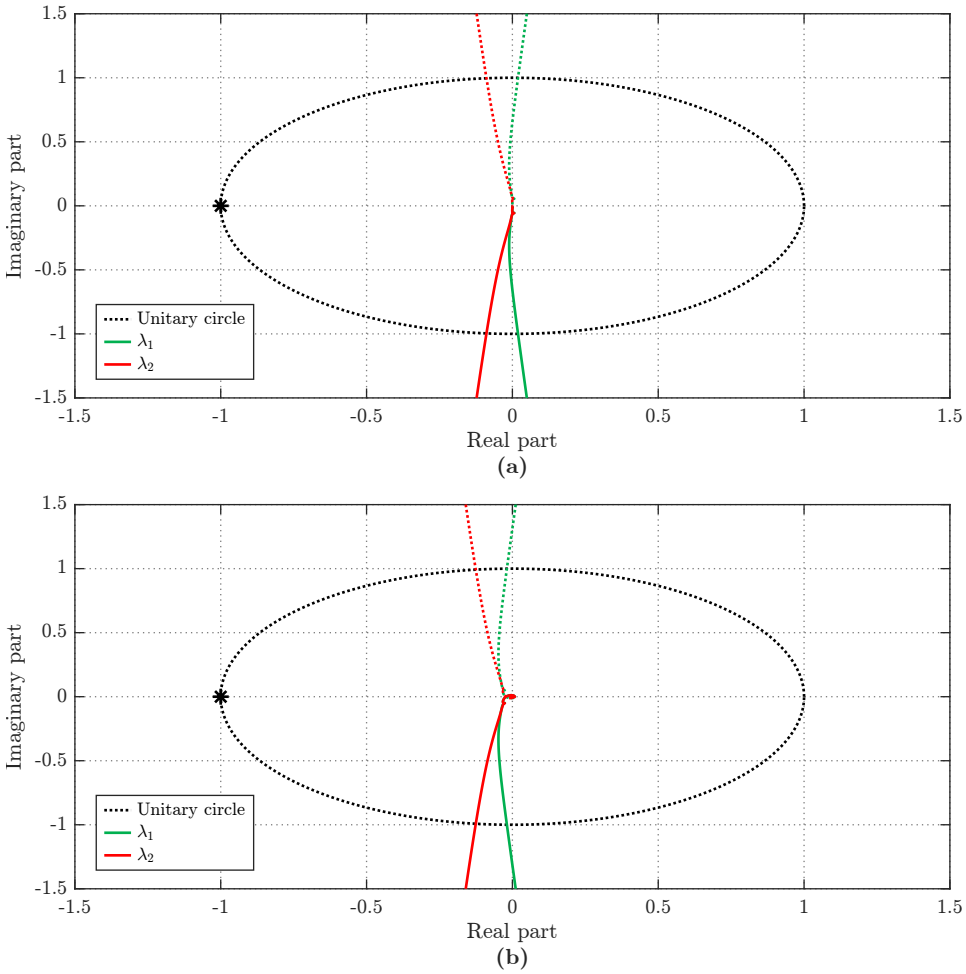


Fig. 3.6. Parallel converter - Nyquist plot of the eigenvalues of the converter current control open loop. **(a)** No delay. **(b)** With delays.

3.5.3 Combined operation

The results presented in Fig. 3.7 show the frequency response of the return ratio, the equivalent parallel admittance, and the inverse of the equivalent series impedance. It can be seen that the inverse of the series impedance is bigger than the parallel admittance, for all frequencies, and also they never cross. The plot of the return ratio shows that is less than unity for all ranges of frequency. The previous results are proved when the complex return ratio is plotted, as shown in the Nyquist plot of Fig. 3.8. It shows no encirclement of the (-1,0). Therefore, the interconnection of the series and parallel converter, designing their controllers utilizing the LQR method, results in a stable and robust system.

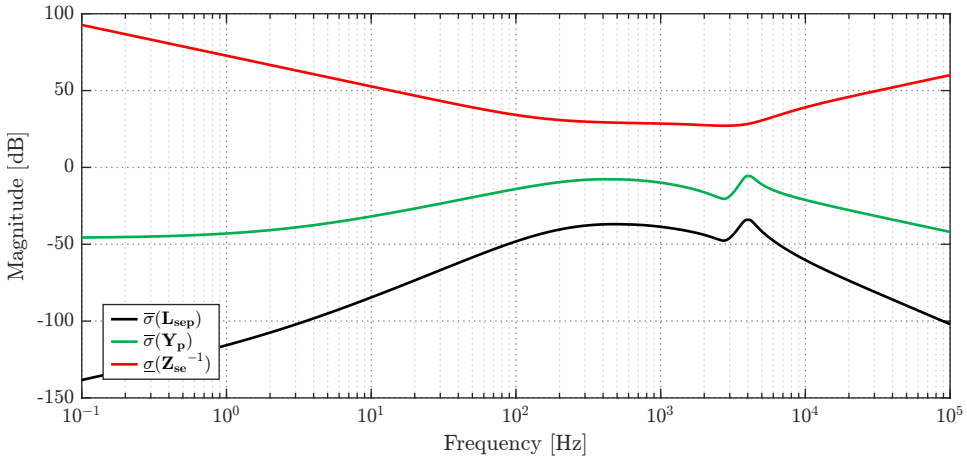


Fig. 3.7. Series and parallel converter - Frequency response.

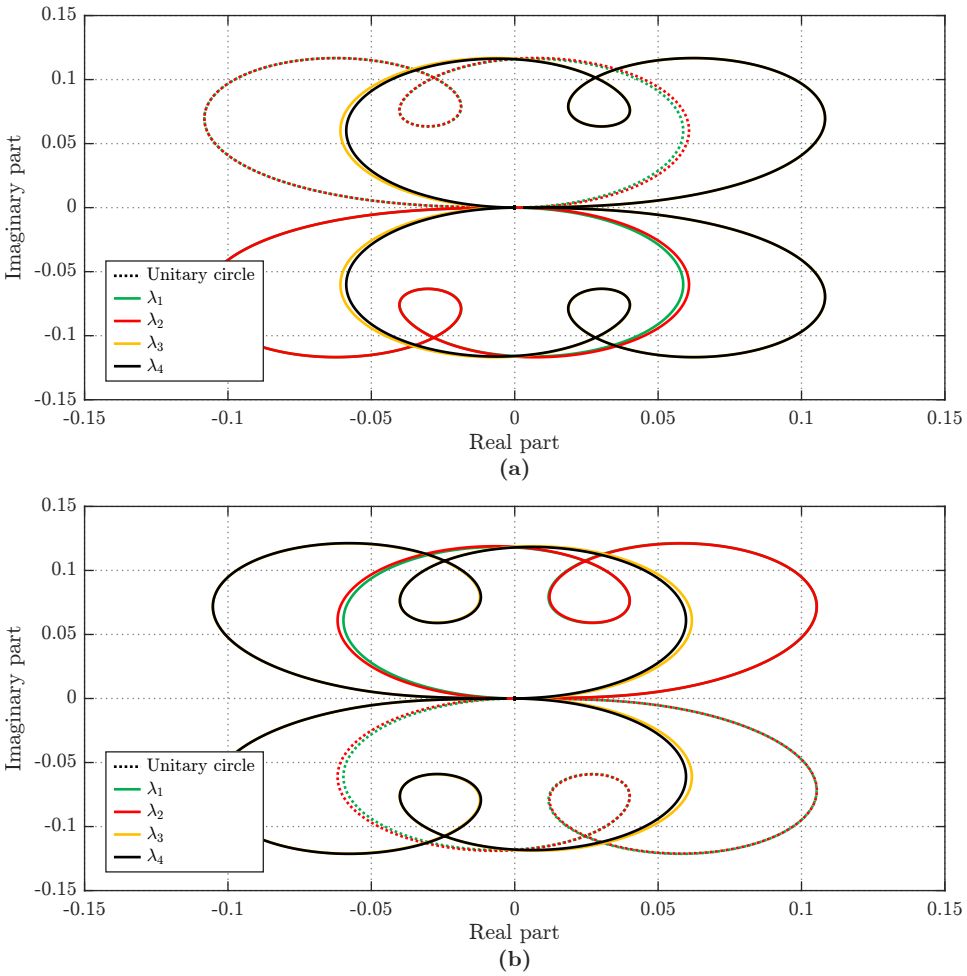


Fig. 3.8. Series and parallel converter - Nyquist plot of the eigenvalues of the combined return ratio. **(a)** No delay. **(b)** With delays.

3.6 Experimental results

In this section, experimental results of the HDT operating under balanced conditions are presented. The diagram of the experimental setup is shown in Fig. B.1 of the **Appendix B**.

The results of Fig. 3.9 present the system response when the parallel and series converter are interconnected through the LFT, and also through the DC-Link. Also, the external control loops, such as the DC-Link controller, grid voltage compensator, and PLLs, are also taken into consideration. Ideally, the system should operate under balanced conditions, nonetheless, the resistive load has internal unbalances, which can be appreciated in the load current.

The results show that during a voltage sag, the HDT is able to inject a series voltage in order to obtain a regulated secondary-side voltage. During this operation, the parallel converter supports the DC-Link voltage by providing the active power demanded by the series converter and compensating the losses. Therefore, the secondary-side current increases during voltage compensation, generating a CAPF. This phenomenon is analyzed in more detail in **Chapter 4**. Additionally, it can be observed that the current of the parallel converter is distorted, which occurs due to the deadtime applied to the modulator, which at the same time is not being compensated. Nonetheless, in **Chapter 5**, this distortion is naturally compensated due to the use of multiresonant current controllers.

The results show that when both power converters are designed independently, the interconnection remains stable when a robust control algorithm, such as LQR. Moreover, after including the external controllers, which are also nonlinear, the stability is preserved, and the HDT operates correctly.

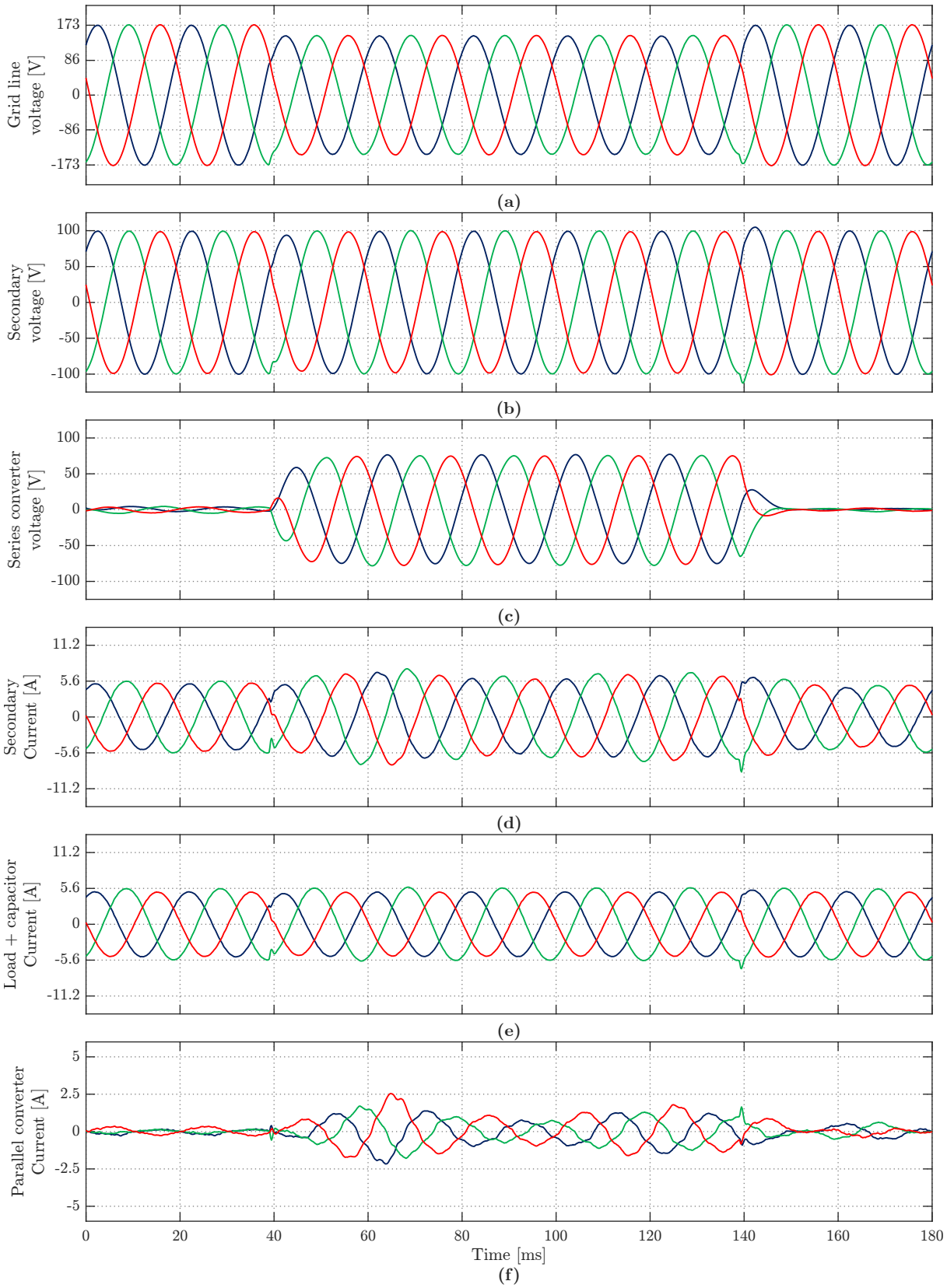


Fig. 3.9. HDT under a balanced voltage sag. **(a)** Grid voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load plus capacitor current. **(f)** Parallel converter current.

3.7 Conclusion

The use of robust control techniques, such as LQR ensures safe gain and phase margin for each controller, preserving the internal stability when both systems are interconnected the stability remains. Moreover, after the system is interconnected and the external control loops such as the DC-Link voltage controller, and grid voltage compensator are taken into consideration, the system remains stable. The DC coupling and the presence of the CAPF do not destabilize the system.

Therefore, in the next chapters, and especially in **Chapter 5**, where the task of the HDT is improving the power quality of the distribution grid, the controllers and estimators design will be based on the LQR.

Chapter 4

CIRCULATING ACTIVE POWER FLOW (CAPF) ANALYSIS AND EFFICIENCY OF THE HDT

Remark: This chapter is partly on the following publications of the author:

[1] A. Carreno, M. Malinowski, M. A. Perez and C. R. Baier, "Circulating Active Power Flow Analysis in a Hybrid Transformer With the Series Converter Connected to the Primary Side," in Early Access of *IEEE Transactions on Industrial Electronics*, 2024.

[2] A. Carreno, M. Malinowski and M. A. Perez, "Circulating Active Power Flow and DC-Link Voltage Ripple in Hybrid Transformers," *IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society*, 2023.

Most HDT configurations comprise two classes of power converters [38]. The first one corresponds to a parallel power converter, which achieves the power balance to regulate

the DC-Link voltage. Moreover, the power converter can improve the PQ by correcting the PF, balancing the load, and acting as an active filter. Typically, they are connected to an AW or the LV side of the LFT [58, 67]. The second converter takes the energy provided by the parallel converter and injects it in series to the grid as a controlled voltage source. Depending on the transformer winding configuration, this operation can be done with or without CTs and connected to the MV or LV side of the LFT [84, 91]. Two HDT configurations can be observed in Fig. 4.1(a)–(b).

Due to the series and parallel converters, the HDT resembles a Unified Power Quality Conditioner (UPQC). Nonetheless, unlike a UPQC, the HDT achieves medium to low voltage transformation. Moreover, thanks to the close interaction of the power converter and LFT, the HDT has additional features, such as:

- The power converter can improve the PQ of the current flowing through the windings of the LFT, which can extend the lifetime of the LFT [92].
- Due to the series connection on the MV side, the HDT can mitigate the voltage disturbances suffered by the LFT, reducing its losses [92].
- During startup, the parallel converter integrated into the HDT can energize the LFT and establish its magnetic flux. Therefore, large inrush currents can be mitigated once connecting to the grid [76, 93].
- The series converter can be utilized to actively modify the magnetic flux of the LFT during voltage disturbances, which can improve the transient response of the LFT by operating in the linear magnetic zone [94].

Additionally, HDTs allow the integration of PV systems [95], and coordinated operation in ADNs [83]. Therefore, the benefits of utilizing an HDT make the HDT a promising solution for the future and more demanding power grids.

Taking into consideration that the HDTs presented in Fig. 4.1(a)–(b) are lossless, the active power processed by the power converters under different voltage sag magnitudes is presented in Fig. 4.1(c). First, for the HDT of Fig. 4.1(a), the active power grows linearly proportional to the voltage sag magnitude. For example, for a 20% voltage sag magnitude, the power converter processes 20% of the load active power. On the other side, for the HDT of Fig. 4.1(b), the behavior of the active power of the converter is nonlinear. Unlike Fig. 4.1(a), this is translated into an increment of the current that flows through the main LFT [96, 97]. Consequently, a CAPF between power converters and the main LFT arises. The relation of the magnitude of the CAPF with respect to

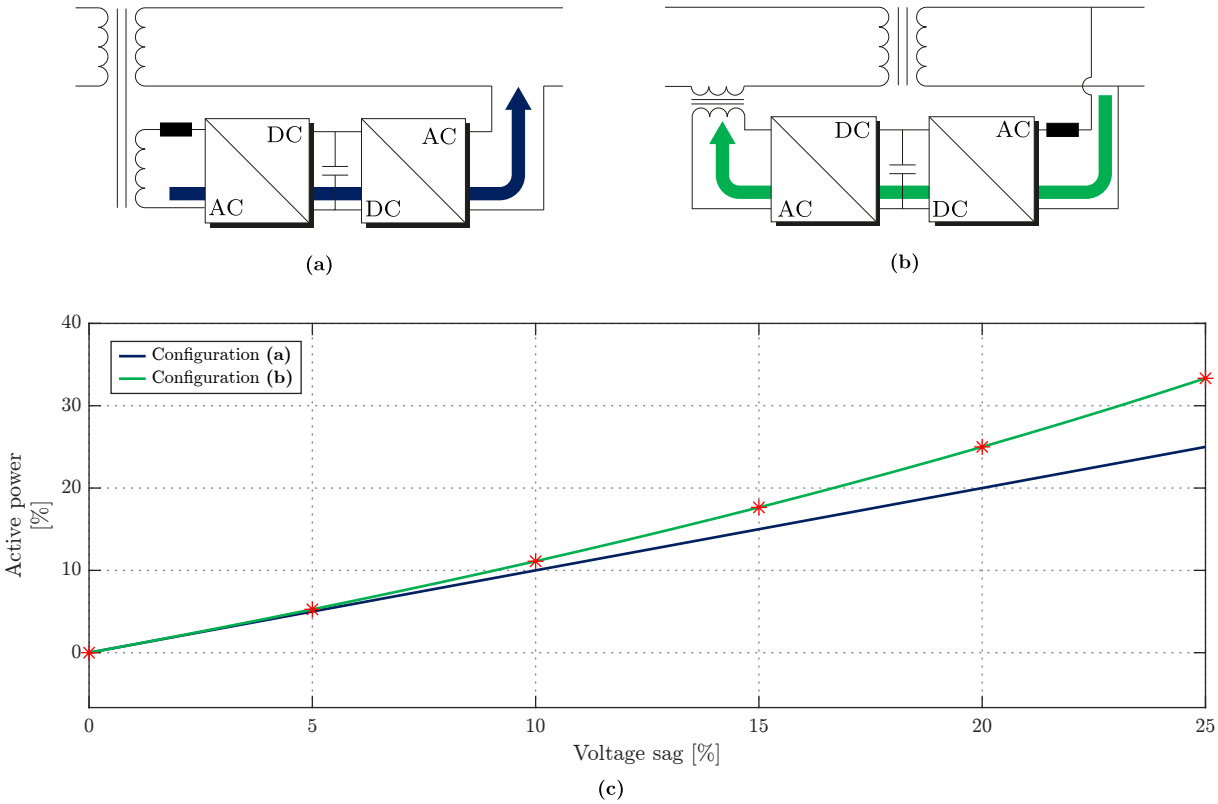


Fig. 4.1. HDT configurations and required active power. **(a)** Series converter connected to the LV side. **(b)** Series converter connected to the MV side. **(c)** Required active power vs. voltage sag magnitude for lossless HDTs.

the grid conditions, power converter, and LFT efficiency has not been researched, as well as the impact on the overall efficiency of the HDT.

Based on the dynamic power balance equations, the power flow characteristics of the HDT have been obtained [98]. The mentioned analysis is done to design a DC-Link controller with good performance under varying grid conditions. Unfortunately, no analysis of CAPF is carried out. Additionally, a power flow analysis has been carried out for an ADN containing HDTs, which also integrate PV generation [99]. Nonetheless, the CAPF phenomenon is not taken into consideration.

Regarding control methods for HDTs, a control algorithm for the series converter based on reactive power injection has been proposed [89]. In this case, no CAPF is observed. Nonetheless, a proper analysis of the operation limits of this control and requirements has yet to be done.

Although the circulating current problem has been researched in different applications, such as the Modular Multilevel Converter [100], parallel connected power converters [101], UPS [102], and DC microgrids [103], the operating conditions that generate the

CAPF phenomenon in HDTs have not been studied yet. The CAPF leads to a worsening of the overall efficiency of the HDT, as well as a worsening of the utilization capability of the power converters. Therefore, this chapter contributes with a detailed analysis of the CAPF of an HDT in which the series converter is connected to the MV side. The analysis considers different operating conditions and how they affect the overall efficiency of the HDT. Moreover, two methods to reduce the CAPF are analyzed: injecting reactive power for voltage control and integrating a BESS into the HDT. To isolate the CAPF phenomenon, only balanced and unbalanced grid and load conditions are considered in this chapter, and the minimum controller required for the operation of the HDT is presented. Nonetheless, an extended controller of the HDT under a polluted grid is presented in **Chapter 5** [92].

4.1 Losses in Distribution Transformers [38]

Transformer losses are composed of load and no-load losses. Load losses depend on the circulating currents generated by the loading of the distribution transformer. The main components are the heat losses in the transformer winding, which are generated by the I^2R term. Stray losses belong to load losses, and they are subdivided as follows: (1) Winding stray losses: losses generated by the effect of leakage electromagnetic flux in the winding. (2) Other stray losses: losses generated by the electromagnetic flux in the core, core clamps, magnetic shields, tank walls, bolts, among others [8].

No-load losses are those generated as a product of the transformer energization to establish the magnetic flux, without loads connected to the transformer winding. No-load losses are composed of the following terms: (1) Hysteresis losses in the core laminations. (2) Eddy current losses in the core laminations. (3) I^2R losses due to the magnetizing current. (4) Dielectric losses [8]. The most relevant are hysteresis and eddy current losses, as they represent almost 99% of the no-load losses. Heat losses due to the magnetizing current are neglected, as magnetizing currents are a small fraction of the rated current of the transformer. In distribution grids applications dielectric losses are neglected as well, as these are relevant when the operating voltages are over 50 kV [104]. The Steinmetz equation is utilized to represent the total core losses under sinusoidal input voltages [105].

$$P_{fe} = K_c f^{\alpha} B_{max}^{\beta} \tag{4.1.1}$$

To cope with the variability of the loads, distribution transformers are designed to operate with maximum efficiency with loading between 40% and 60%. Above that,

the efficiency starts to decrease due to the winding losses. On the other hand, under low loading operating, core losses are predominant, leading to a poor and unsustainable operation [106]. For example, for a 1000 kVA distribution transformer operating with unit PF, the efficiency at 10% 45% and 100% load are 96.99%, 98.70%, and 98.37%, respectively. The efficiency is worsened under different grid conditions, such as low PF [107]. In light-load scenarios, the power converters of the HDT can be utilized to improve the efficiency [23].

The applied voltage magnitude has a critical impact on the insulation materials of the transformer, as high $\mathrm{d}v/\mathrm{d}t$ can create high electric fields. In the presence of distorted grid voltages, the dv/dt increases, accelerating the degradation of the insulation materials and reducing the transformer lifetime [90]. In [104], different nonlinear voltage profiles have been studied and it is shown that they have a drastic impact on the transformer no-load losses, and increase the maximum flux density of the magnetic core. Furthermore, the magnetic flux inside the core is nonuniform, which generates partial saturation, and temperature rise, among other issues. In [9], a distribution transformer is tested under different operating regimes. In the case of a line-to-line voltage THD of about 12%, the no-load losses and no-load current increase in about 3.46% and 37.3% compared to a sinusoidal voltage. The work in [10] analyzes the effect of grid voltage harmonics on the distribution transformer performance. Some results show that the core losses increase by about 21% when the voltage harmonics are given by the worst-case scenario of the harmonics limits given by IEC 61000-3-6. Additionally, the results of the impact of third and fifth harmonics on the temperature of the transformer are presented. Compared to a pure sinusoidal voltage, there is an 8.2% and 11.8% temperature increase of the hottest spot, for 3% of third and fifth harmonics. The system presents higher losses as the frequency increases due to the effect of temperature and skin effect on the winding resistance.

Compared to voltage harmonics, load harmonics have a bigger impact on the transformer losses and lifetime [108]. The study of load harmonics and the effect on the transformer is crucial for the transformer design, as it gives guidance for its derating. The IEEE std C57.110 establish recommended practices for liquid-filled and dry-type transformer when supplying non-linear loads. Among the load losses, winding stray losses depend on the square of the frequency, while the exponent of other stray losses is less than one. When a transformer operates supplying nonlinear currents, the additional winding stray losses increase the hot-spot temperature [8]. The rise in the temperature affects the insulation systems, reducing the lifetime of the transformer. The hot-spot temperature (θ_H), can be utilized to calculate the aging acceleration factor (F_{AA}), which,

for a mineral-oil immersed transformer, is given as follows [109].

$$\theta_H = \theta_A + \Delta\theta_{To} + \Delta\theta_H \tag{4.1.2}$$

$$F_{AA} = e^{\frac{15000}{110+273} - \frac{15000}{\theta_H+273}} \tag{4.1.3}$$

where θ_A is the ambient temperature, $\Delta\theta_{To}$ is the oil temperature rise over the ambient temperature, and $\Delta\theta_H$ is the winding hot-spot temperature rise over the top oil temperature.

In [110] a load characterized by consuming high fifth and seventh harmonics is analyzed utilizing three different methods to calculate the transformer losses and estimated lifetime. Under the analyzed operating conditions, the minimum F_{AA} is equal to 1.12, which for a transformer with an expected operating time of 30 years, the lifetime is decreased in a 10%. In [111], a load current profile given by 5%, 6%, and 5% for the third, fifth and seventh harmonic is tested. Under these operating conditions, the core losses increase by about 15.5%, with respect to a full sinusoidal case [111].

4.2 CAPF model

To obtain the mathematical model of the CAPF, first, the model of the HDT in *abc* coordinates presented in Fig. 4.2(a) is transformed to an equivalent model in $\alpha\beta$ coordinates, shown in Fig. 4.2(b). The common mode current component, γ, is not considered during the analysis due to the configuration of the transformer removes their effect.

Main LFT and power converter stage

The following expressions give the instantaneous active power of the grid, series converter, parallel converter, and load.

$$p_g = v_{g\alpha\beta} \cdot i_{g\alpha\beta} = P_g + \widetilde{p}_g \tag{4.2.1a}$$

$$p_{se} = v_{se\alpha\beta} \cdot i_{g\alpha\beta} = P_{se} + \widetilde{p}_{se} \tag{4.2.1b}$$

$$p_p = v_{s\alpha\beta} \cdot i_{p\alpha\beta} = P_p + \widetilde{p}_p \tag{4.2.1c}$$

$$p_L = v_{s\alpha\beta} \cdot i_{L\alpha\beta} = P_L + \widetilde{p}_L \tag{4.2.1d}$$

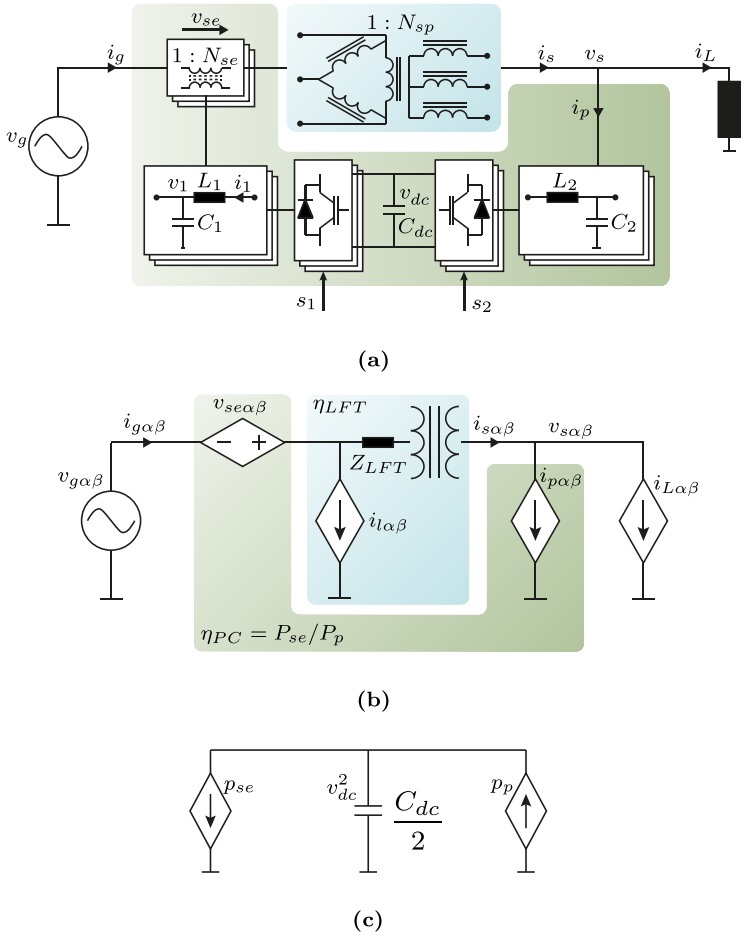


Fig. 4.2. HDT model to for CAPF analysis. **(a)** Simulation/Experimental diagram. **(b)** Simplified model in $\alpha\beta$ coordinates. **(c)** DC-Link energy model.

where $(P_g, \widetilde{p}_g)$, $(P_{se}, \widetilde{p}_{se})$, $(P_p, \widetilde{p}_p)$, $(P_L, \widetilde{p}_L)$ are the average and oscillatory active power components of the grid, series converter, parallel converter, and load. The grid current, $i_{g\alpha\beta}$, is given as follows.

$$i_{g\alpha\beta} = N_{sp}(i_{L\alpha\beta} + i_{p\alpha\beta}) + i_{l\alpha\beta} \tag{4.2.2}$$

Regarding the simplified model, the LFT is modeled with a series impedance that concentrates the copper losses and the leakage inductance, given as follows.

$$Z_{LFT} = R_{LFT} + jX_{LFT} \tag{4.2.3}$$

where R_{LFT} and X_{LFT} represent the copper losses and leakage reactance, respectively. To simplify the following analysis, the remaining losses of the LFT are concentrated and modeled by a parallel current source, i_l, that consumes a power equal to P_l. For modeling

purposes, i_l does not contribute to the series voltage drop of the LFT. The efficiency of the LFT, measured from the primary to secondary side, is given by η_{LFT}.

The series stage comprises a series voltage-controlled source, whose output is $v_{se\alpha\beta}$, whereas the parallel converter is modeled as a current source, whose output is $i_{p\alpha\beta}$. Both controlled sources are interconnected through the DC-Link, which is assumed to be balanced. Therefore, the active power balance must be kept between them. The efficiency of the power converter stage is given by η_{PC}, which also contains the efficiency of the CTs according to Fig. 4.2. The following equations define the efficiency of the LFT and power converter stage.

$$\eta_{LFT} = \frac{P_s}{P_p} \tag{4.2.4a}$$

$$\eta_{PC} = \frac{P_{se}}{P_p} \tag{4.2.4b}$$

Grid and load voltage

The CAPF is generated when the HDT is employed to mitigate the grid voltage disturbances. The following equation models the grid voltage for balanced and unbalanced conditions.

$$v_{g\alpha\beta} = (1 - K_{vp})|V_n|\hat{x} + K_{vn}|V_n|\hat{x}_{vn} \tag{4.2.5}$$

where $|V_n|$ represents the nominal voltage of the grid, and K_{vp} represents the balanced deviation from the nominal grid voltage magnitude. K_{vp} describes the balanced grid voltage component as follows.

$$K_{vp}\begin{cases} < 0, & \text{for a grid voltage swell} \\ > 0, & \text{for a grid voltage sag} \\ = 0, & \text{nominal grid voltage} \end{cases} \tag{4.2.6}$$

The parameter K_{vn} models the ratio of negative sequence in the grid voltage with respect to the nominal grid voltage. The unitary vectors containing the positive sequence and negative sequence phases of the grid voltage are given as follows.

$$\hat{x} = \begin{bmatrix} \cos(\theta) \\ \sin(\theta) \end{bmatrix} \tag{4.2.7a}$$

$$\hat{x}_{vn} = \begin{bmatrix} \cos(\theta + \phi_{vn}) \\ -\sin(\theta + \phi_{vn}) \end{bmatrix} \tag{4.2.7b}$$

where $\theta = \omega t$ corresponds to the phase of the positive-sequence component of the grid voltage, and ϕ_{vn} is the negative sequence phase-shift. Considering the controller action of the series converter and neglecting the winding configuration of the main LFT, the secondary side voltage is regulated to its nominal value, preserving the angle of the grid. Therefore, the following secondary-side voltage is obtained.

$$v_{s\alpha\beta} = N_{sp}|V_n|\hat{x} \tag{4.2.8}$$

Note that the latter is only valid when utilizing the conventional controller for the series converter. It will be shown later that the controller of the series converter can be modified to reduce the CAPF. In this scenario, the angle of the grid voltage is not maintained.

Load current

According to Fig. 4.2(b), the load is modeled as a controlled current source and is given by the following equation.

$$i_{L\alpha\beta} = \underbrace{I_L\hat{x}}_{\substack{\text{Balanced} \\ \text{active} \\ \text{component}}} + \underbrace{K_{iq}I_L\hat{x}_q}_{\substack{\text{Balanced} \\ \text{reactive} \\ \text{component}}} + \underbrace{K_{in}I_L\hat{x}_{in}}_{\substack{\text{Unbalanced} \\ \text{component}}} \tag{4.2.9}$$

The load current has three components. The first corresponds to the active balanced component, in which I_L represents the magnitude of the active current consumed/injected by the load. The second one corresponds to the reactive current, where K_{iq} indicates the proportion of reactive power with respect to the active current. Lastly, The unbalanced component is parametrized by K_{in}, which represents the proportion of negative sequence current with respect to the active component. All components are written in terms of the active current because this is what originates the CAPF. Therefore, it is always assumed that the load at least consumes or generates active power. The reactive and negative sequence unitary vectors of the load are given as follows.

$$\hat{x}_q = \begin{bmatrix} \cos(\theta - \pi/2) \\ \sin(\theta - \pi/2) \end{bmatrix} \tag{4.2.10a}$$

$$\hat{x}_{in} = \begin{bmatrix} \cos(\theta + \phi_{in}) \\ -\sin(\theta + \phi_{in}) \end{bmatrix} \tag{4.2.10b}$$

where ϕ_{in} is the phase shift of the negative sequence load current with respect to the balanced components.

Parallel converter current

On one side, the parallel converter serves as a support unit for the series converter, i.e., it delivers the active power required during its operation. On the other side, the parallel converter is utilized to improve the quality of the secondary-side currents, which in this chapter corresponds to reactive power and negative sequence compensation. Therefore, the parallel converter current is decomposed as follows.

$$i_{p\alpha\beta} = \underbrace{I_p \hat{x}}_{\substack{\text{Balanced} \\ \text{active} \\ \text{component}}} - \underbrace{T_{iq} K_{iq} I_L \hat{x}_q}_{\substack{\text{Balanced} \\ \text{active} \\ \text{component}}} - \underbrace{T_{in} K_{in} I_L \hat{x}_{in}}_{\substack{\text{Balanced} \\ \text{active} \\ \text{component}}} \tag{4.2.11}$$

where I_p corresponds to the magnitude of the active component, which depends on the compensation level provided by the series converter and the power converter efficiency. This component is so far unknown. On the other side, the additional introduced parameters, given by T_{iq} and T_{in}, regulate the amount of compensation the parallel converter provides for the reactive and negative sequence components.

Series converter voltage

The injected series voltage is utilized to mitigate the disturbances presented on the grid voltage and provide nominal voltage on the secondary side. Therefore, the injected voltage, v_{se}, is given as follows.

$$v_{se\alpha\beta} = \underbrace{K_{vp}|V_n|\hat{x}}_{\substack{\text{Balanced} \\ \text{component} \\ \text{compensation}}} - \underbrace{K_{vn}|V_n|\hat{x}_{nv}}_{\substack{\text{Unbalanced} \\ \text{component} \\ \text{compensation}}} + \underbrace{N_{sp} Z_{LFT}(i_{p\alpha\beta} + i_{L\alpha\beta})}_{\substack{\text{Voltage} \\ \text{drop} \\ \text{compensation}}} \tag{4.2.12}$$

The series voltage has the following components:

1. A balanced component mitigates the balanced grid voltage sag/swell. This voltage has the same phase angle as the positive sequence of the grid voltage.
2. The unbalanced component of the grid voltage shifted in 180 degrees.
3. The internal voltage drop of the LFT.

The components 1. and 2. provide a balanced and nominal voltage on the terminals of the MV side of the main LFT. The current of component 3. corresponds to the summation of the load and parallel converter current, which flows through the equivalent series impedance of the LFT. By injecting (4.2.12), a nominal and balanced voltage is obtained on the load terminal.

CAPF calculation

According to the simplified model, the injected voltage is given by the following equation when the series converter regulates the secondary-side voltage to its rated value.

$$v_{se\alpha\beta} = K_{vp}|V_n|\hat{x} - K_{vn}|V_n|\hat{x}_{vn} + L_{LFT}N_{sp}\frac{\mathrm{d}(i_{p\alpha\beta} + i_{L\alpha\beta})}{\mathrm{d}t} + R_{LFT}N_{sp}(i_{p\alpha\beta} + i_{L\alpha\beta}) \quad (4.2.13)$$

Then, the instantaneous active power of the series converter is given by the dot product between the series voltage and the grid current.

$$\begin{aligned} p_{se} = v_{se\alpha\beta} \cdot i_{g\alpha\beta} = \quad & \underbrace{K_{vp}|V_n|\hat{x} \cdot i_{g\alpha\beta}}_{①} \underbrace{-K_{vn}|V_n|\hat{x}_{vn} \cdot i_{g\alpha\beta}}_{②} + \underbrace{L_{LFT}N_{sp}\frac{\mathrm{d}(i_{p\alpha\beta} + i_{L\alpha\beta})}{\mathrm{d}t} \cdot i_{g\alpha\beta}}_{③} \\ & + \underbrace{R_{LFT}N_{sp}(i_{p\alpha\beta} + i_{L\alpha\beta}) \cdot i_{g\alpha\beta}}_{④} \end{aligned} \quad (4.2.14)$$

Under the stated operating conditions, the solution for each one of the components of the instantaneous active power of the series converter is given below.

$$\begin{aligned} ① = \quad & K_{vp}N_{sp}|V_n|(I_L + I_p) + K_{vp}|V_n|I_l \\ & + K_{vp}N_{sp}|V_n|K_{in}(1 - T_{in})I_L\cos(\theta_{in}) \end{aligned} \quad (4.2.15a)$$

$$
\begin{aligned}
\textcircled{2} = \quad & -K_{vn}N_{sp}|V_n|K_{in}(1-T_{in})I_L\cos(\phi_{vin}) \\
& - K_{vn}|V_n|\left[N_{sp}(I_L+I_p)+I_l\right]\cos(\theta_{vn}) - K_{vn}N_{sp}|V_n|K_{iq}(1-T_{iq})I_L\sin(\theta_{vn})
\end{aligned} \tag{4.2.15b}
$$

$$
\begin{aligned}
\textcircled{3} = \quad & \omega N_{sp}L_{LFT}K_{iq}(1-T_{iq})I_LI_l \\
& - 2\omega N_{sp}^2L_{LFT}(I_p+I_L)K_{in}(1-T_{in})I_L\sin(\theta_{in}) \\
& + 2\omega N_{sp}^2L_{LFT}K_{iq}(1-T_{iq})K_{in}(1-T_{in})I_L^2\cos(\theta_{in}) - \omega N_{sp}L_{LFT}K_{in}(1-T_{in})I_LI_l\sin(\theta_{in})
\end{aligned} \tag{4.2.15c}
$$

$$
\begin{aligned}
\textcircled{4} = \quad & R_{LFT}[N_{sp}^2(I_p+I_L)^2 + N_{sp}(I_p+I_L)I_l + N_{sp}^2K_{iq}^2(1-T_{iq})^2I_L^2 \\
& + N_{sp}^2K_{in}^2(1-T_{in})^2I_L^2] \\
& + R_{LFT}[N_{sp}^2(I_p+I_L)K_{in}(1-T_{in})I_L\cos(\theta_{in}) + N_{sp}^2K_{iq}(1-T_{iq})K_{in}(1-T_{in})I_L^2\sin(\theta_{in}) \\
& + N_{sp}^2K_{in}(1-T_{in})I_L(I_L+I_p)\cos(\theta_{in}) + N_{sp}K_{in}(1-T_{in})I_LI_l\cos(\theta_{in}) \\
& + N_{sp}^2K_{in}(1-T_{in})K_{iq}(1-T_{iq})I_L^2\sin(\theta_{in})]
\end{aligned} \tag{4.2.15d}
$$

On the other side, the instantaneous active power of the parallel converter is given as follows.

$$
p_p = v_{s\alpha\beta}\cdot i_{p\alpha\beta} = N_{sp}|V_n|I_p - N_{sp}|V_n|K_{in}T_{in}I_L\cos(\theta_{in}) \tag{4.2.16}
$$

where the terms marked in cyan correspond to the DC components of the instantaneous active power of the series and parallel converters.

According to the simplified model, the equivalent parallel losses of the main LFT do not directly contribute to the voltage drop of the transformer. Nonetheless, they circulate through the series converter, contributing to the overall losses of the HDT. The following average active power definitions for the load, parallel converter, and other transformer losses will be considered:

$$
P_L = N_{sp}|V_n|I_L \tag{4.2.17a}
$$

$$
P_p = N_{sp}|V_n|I_p \tag{4.2.17b}
$$

$$
P_l = |V_n|I_l \tag{4.2.17c}
$$

Then, the average active power of the series converter, P_{se}, is obtained below.

$$P_{se} = \underbrace{N_{sp}^2 R_{LFT}\left[(I_p + I_L)^2 + K_{iq}^2(1-T_{iq})^2 I_L^2 + K_{in}^2(1-T_{in})^2 I_L^2\right]}_{P_{Cu}} + K_{vp}(P_p + P_L + P_l)$$
$$- K_{vn}K_{in}(1-T_{in})\cos(\phi_{vin})P_L + \frac{R_{LFT}}{|V_n|^2}P_l(P_p + P_L) + \frac{\omega L_{LFT}K_{iq}(1-K_{iq})}{|V_n|^2}P_l P_L \tag{4.2.18}$$

where ϕ_{vin} is the phase shift between the negative sequence voltage and current, given as follows.

$$\phi_{vin} = \phi_{vn} - \phi_{in} \tag{4.2.19}$$

Regarding (4.2.18), the copper losses of the transformer, represented by P_{Cu}, can be written in terms of the efficiency of the LFT. After obtaining the average active power on the input and output of the transformer and following a similar approach as before, the copper losses are shown below.

$$P_{Cu} = \frac{1-\eta_{LFT}}{\eta_{LFT}}(P_p + P_L) - P_l - \frac{R_{LFT}}{|V_n|^2}P_l(P_p + P_L) - \frac{\omega L_{LFT}K_{iq}(1-K_{iq})}{|V_n|^2}P_l P_L \tag{4.2.20}$$

After replacing the copper losses into (4.2.18), the following equation that relates the active power balance of the power converter stage is obtained.

$$\begin{aligned}\eta_{PC}P_p &= P_{se}\\ \eta_{PC}P_p &= \frac{1-\eta_{LFT}}{\eta_{LFT}}(P_p + P_L) + K_{vp}(P_p + P_L + P_l) - K_{vn}K_{in}(1-T_{in})\cos(\phi_{vin})P_L - P_l\end{aligned} \tag{4.2.21}$$

where η_{LFT} depends on the operating conditions of the LFT, including the effects of the losses due to the reactive and negative sequence currents and remaining losses of the transformers, P_l. Then, by solving the power balance (4.2.21), the active power of the parallel converter, i.e., the CAPF, is obtained.

$$P_p = \underbrace{\frac{K'_{vp}}{1-K'_{vp}}P_L}_{①} - \underbrace{\frac{K'_n}{1-K'_{vp}}P_L}_{②} - \underbrace{\alpha_P}_{③} \tag{4.2.22}$$

The CAPF has three distinctive components. The first one, labeled as ①, depends on the interaction of the balanced components of the system. The parameter K'_{vp} represents the equivalent voltage sag/swell of the system, i.e. the grid voltage sag/swell plus the additional sag/swell due to the internal losses of the transformer. K'_{vp} is defined given below.

$$K'_{vp} = \frac{1-\eta_{LFT}+\eta_{LFT}K_{vp}}{\eta_{LFT}\eta_{PC}} \tag{4.2.23}$$

The second component, labeled as ②, represents the effect of the interaction of the negative sequence of the grid voltage and the uncompensated negative sequence of the load current on the CAPF. The parameter K'_n is the equivalent negative sequence interaction factor, given as follows.

$$K'_n = \frac{K_n}{\eta_{PC}} = \frac{K_{vn}K_{in}(1-T_{in})\cos(\phi_{vin})}{\eta_{PC}} \tag{4.2.24}$$

When the series converter compensates for the negative sequence presented on the grid voltage and, and the same time uncompensated unbalanced components of the load current circulate through the MV side, their interaction will generate active power. The previous active power will contribute to the CAPF.

Finally, the component labeled as ③, corresponding to α_P, includes the effect of the equivalent parallel losses of the transformer on the CAPF. α_P is given as follows.

$$\alpha_P = \frac{1-K_{vp}}{\eta_{PC}(1-K'_{vp})}P_l \tag{4.2.25}$$

Note that if α_P or P_l are not considered in (4.2.22), it would be assumed that all the active power flows through the series impedance, resulting in a larger voltage drop. Consequently, the resulting CAPF would be larger, leading to incorrect efficiency results.

The relationship of the CAPF with respect to the balance sag/swell proportion, K_{vp}, and when the system losses are neglected, is shown in Fig. 4.3(a). In this scenario, the CAPF shown in (4.2.22) is simplified as follows.

$$P_p = \frac{K_{vp}}{1-K_{vp}}P_L \tag{4.2.26}$$

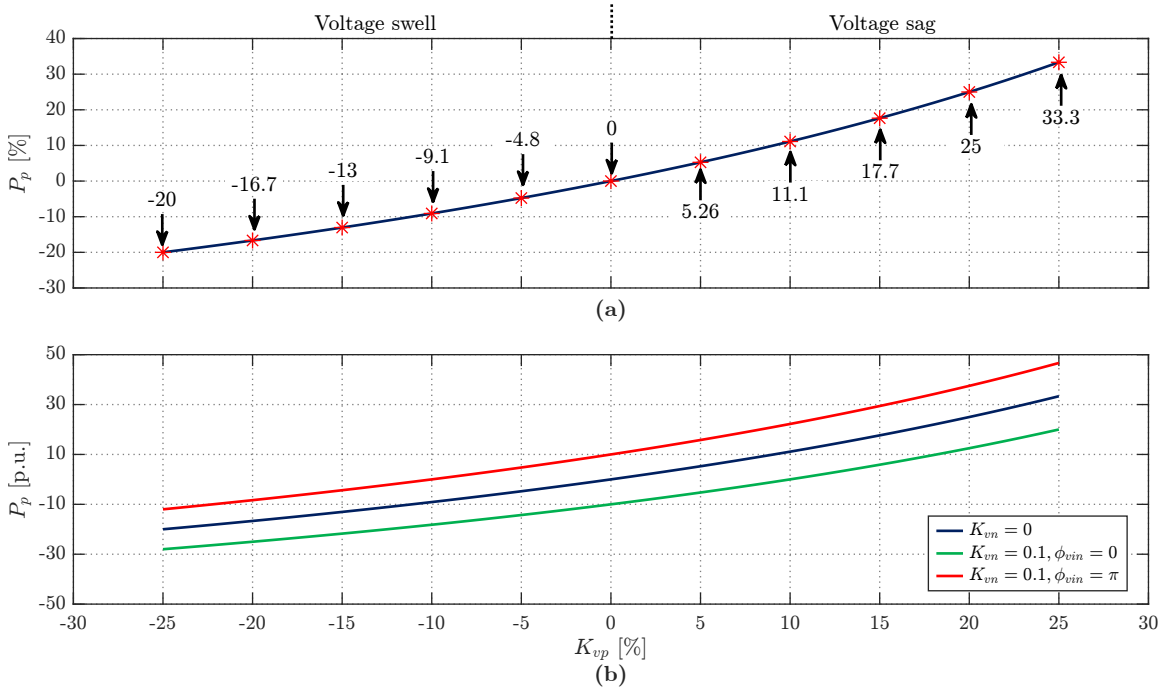


Fig. 4.3. Ideal steady-state CAPF behavior. **(a)** CAPF for balanced grid conditions. **(b)** CAPF for unbalanced grid conditions.

It can be seen that for voltage sags ($K_{vp} > 0$), there is a positive CAPF, whereas for voltage swells ($K_{vp} < 0$), the CAPF is negative. If the grid voltage disturbance corresponds to a sag or swell, the power that the LFT processes will increase or decrease, respectively. It can be seen that in order to compensate for a 10% voltage sag, the power converter needs to process 11% of the load active power. A more demanding scenario occurs when the power HDT compensates for a 25% voltage sag, which requires processing 33% of the load active power. Therefore, under high-load operation, the additional CAPF required to compensate for the voltage sags could overload the LFT. The opposite occurs, for example, under a 25% voltage swell, in which the power converters need to process 20% of the load active power. Nonetheless, this additional power is subtracted from the LFT, and no overload occurs. As the LFT and the power converters are ideal, the HDT efficiency is 100%, and the CAPF just circulates between the LFT and power converter without generating additional losses.

The effect of the negative sequence grid voltage and load current interaction in the CAPF is shown in the Fig. 4.3(b). When the losses are neglected in (4.2.22), the following is obtained.

$$P_p = \frac{K_{vp}}{1 - K_{vp}} P_L - \frac{K_{vn} K_{in} \cos(\phi_{vin})}{1 - K_{vp}} P_L \tag{4.2.27a}$$

$$P_p = \frac{K_{vp} - K_{vn}K_{in}\cos(\phi_{vin})}{1 - K_{vp}} P_L \tag{4.2.27b}$$

It can be observed that an additional term given by $K_{vn}K_{in}\cos(\phi_{vin})$ is present. This term corresponds to the ideal active power injected by the series converter originated by the negative sequence voltage and current. Then, this additional power is augmented due to the power circulation, represented by $1-K_{vp}$ in the denominator. The additional term, depending on the phase relation of $\cos(\phi_{vin})$, can be additive or subtractive. Fig. 4.3(b) shows the resulting CAPF when the phase relation variates between $\pm\pi$. Note that connecting the same load between different phases of the secondary side will generate the same amplitude for the negative sequence current but different phase angles. Therefore, the resulting CAPF will increase or decrease depending on how the equivalent load is connected. This is shown in an example next.

Fig. 4.4 shows a simplified representation of the CAPF for different grid and load conditions. According to (4.2.22), in the presence of voltage sags, a positive CAPF will be required. The CAPF will be added to the load power flow, increasing the LFT active power. On the other side, a reverse power flow is obtained under a voltage swell, which decreases the active power through the LFT. Nonetheless, in the case of grid and load unbalances, an additional CAPF is obtained, which can be additive or subtractive depending on the phase relation of the negative sequence of the grid voltage and load current.

4.2.1 Comments on ϕ_{vin} and CAPF example

In this chapter, the simplified model neglects the phase shift introduced by the $\Delta - Y$ transformer and only considers its turn ratio. Nonetheless, in order to calculate ϕ_{vin}, the rotation angle must be taken into consideration.

Considering the positive and negative sequence components of the primary-side voltage and secondary-side current of the LFT, and applying the matrix transformations of (2.4.9) and (2.4.15), the following applies:

- There is a phase shift of $\pi/6$ rad when transferring the positive sequence voltage from the MV to the LV side.
- There is a phase shift of $-\pi/6$ rad when transferring the negative sequence voltage from the MV to the LV side.
- There is a phase shift of $-\pi/6$ rad when transferring the positive sequence current from the LV to the MV side.

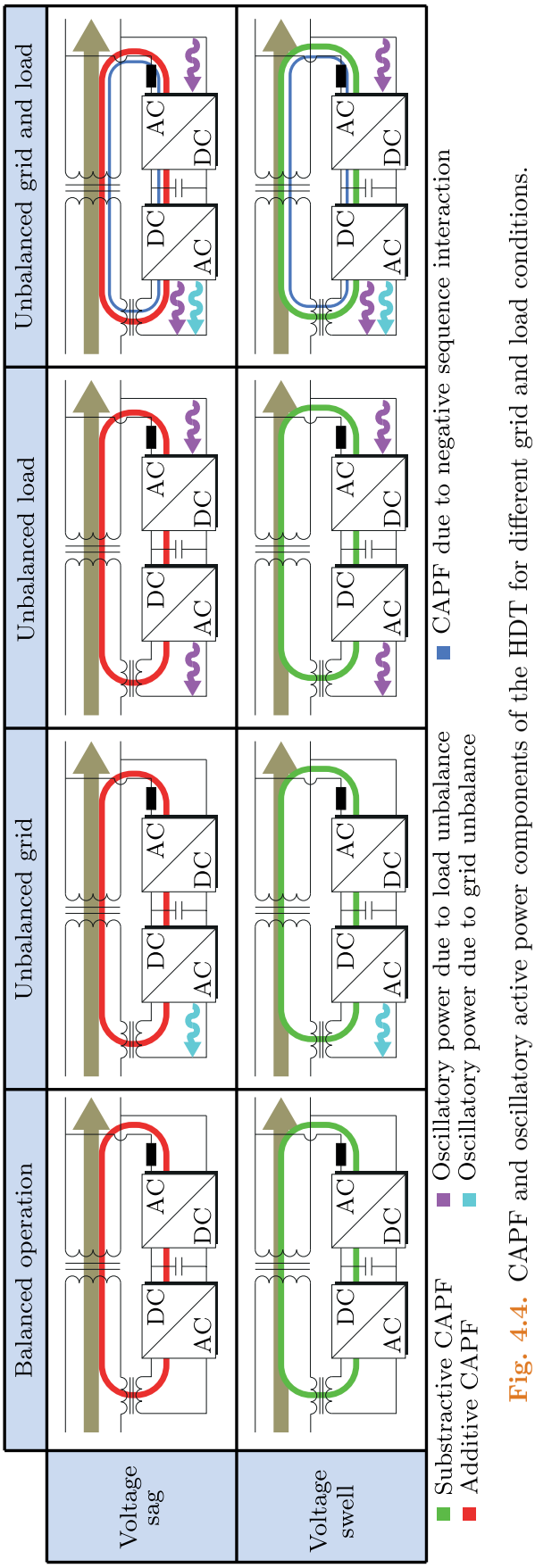


Fig. 4.4. CAPF and oscillatory active power components of the HDT for different grid and load conditions.

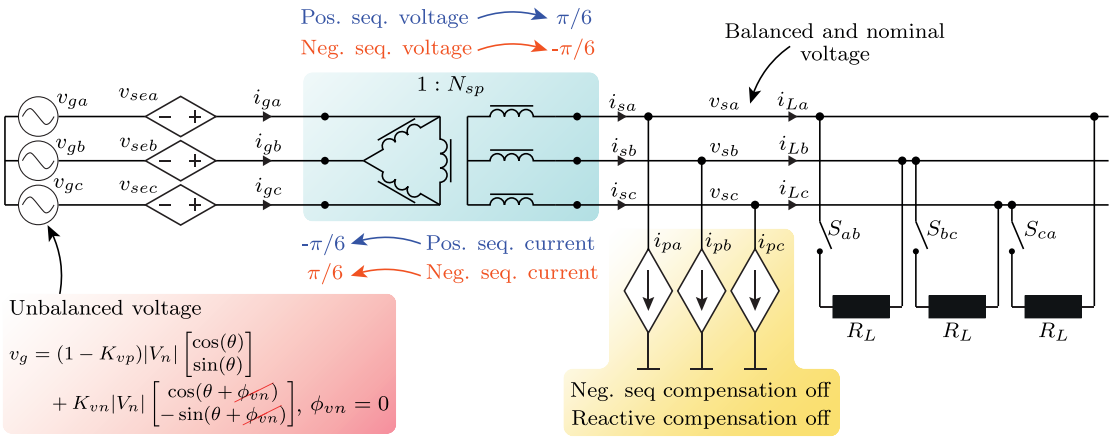


Fig. 4.5. CAPF example under unbalanced load.

- There is a phase shift of $\pi/6$ rad transferring the positive sequence current from the LV to the MV side.

Therefore, in all operations during this chapter, a phase shift of $\pi/6$ rad must be applied to the negative sequence that exists on the secondary side. Moreover, the reference node of all the voltages and currents is the grid voltage, and typically the negative sequence phase is given with respect to the positive sequence voltage of its own node, i.e., the secondary side node. Therefore, the phase shift due to the positive sequence voltage due to the LFT must be considered, increasing the total phase shift to $\pi/3$ rad.

Example Case

An example circuit to analyze the effect of load unbalances on the CAPF is shown in Fig. 4.5. In this system, the grid voltage has balanced and unbalanced components, but as usual, the series converter regulates them, and only positive sequence with nominal magnitude is present on the secondary side. On the other side, the load is composed of three resistors, which are activated by the switches S_{ab}, S_{bc}, and S_{ca}. The parallel converter compensation is neglected for these purposes, and therefore the reactive and negative sequence compensation are turned off, i.e., $T_{iq} = 0$ and $T_{in} = 0$. The load current is modeled in terms of its phasor representation as follows.

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \frac{S_{ab}}{R_L} \begin{bmatrix} 1 & -1 & 0 \\ -1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} + \frac{S_{bc}}{R_L} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & -1 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} + \frac{S_{ca}}{R_L} \begin{bmatrix} 1 & 0 & -1 \\ 0 & 0 & 0 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{4.2.28}$$

The load voltage phasor, with a phase shift equal to zero, is written as follows.

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = N_{sp}|V_n| \begin{bmatrix} 1 \\ \alpha^2 \\ \alpha \end{bmatrix} \tag{4.2.29}$$

where

$$\alpha = e^{\frac{2\pi}{3}j} \tag{4.2.30}$$

Then, taking the inverse Fortescue transformation, the zero, positive, and negative sequences of the load current in terms of its phasor are obtained as follows.

$$\begin{bmatrix} I_{L_0} \\ I_{L_+} \\ I_{L_-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \tag{4.2.31}$$

Then premultiplying (4.2.28) by the inverse Fortescue transformation and writing the secondary-side voltage in terms of its phasors, the zero, positive, and negative sequence components of the load current are given as follows.

$$\begin{bmatrix} I_{L_0} \\ I_{L_+} \\ I_{L_-} \end{bmatrix} = \frac{N_{sp}|V_n|S_{ab}}{R_L} \begin{bmatrix} 0 \\ 1 \\ 1/2 + j\sqrt{3}/2 \end{bmatrix} + \frac{N_{sp}|V_n|S_{bc}}{R_L} \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} + \frac{N_{sp}|V_n|S_{ca}}{R_L} \begin{bmatrix} 0 \\ 1 \\ 1/2 - j\sqrt{3}/2 \end{bmatrix} \tag{4.2.32}$$

From the previous equation, it can be observed that for each scenario the positive sequence current remains unchanged, and therefore the average active power of the load is the same for each scenario. The previous is consistent because independently of the phases to which a resistor is connected, the amount of active power consumed will be the same only if the voltages are perfectly balanced. The latter occurs thanks to the series converter, which balances and regulates the load voltage. On the other side, the magnitude of the negative sequence is also the same for each scenario. Nonetheless, its phase shift changes.

$$I_{L+} = \frac{N_{sp}|V_n|}{R_L} \quad , \quad (S_{ab}, S_{bc}, S_{ca}) = (1,0,0) \quad \text{or} \quad (0,1,0) \quad \text{or} \quad (0,0,1) \tag{4.2.33}$$

$$|I_{L-}| = \frac{N_{sp}|V_n|}{R_L} \quad , \quad (S_{ab}, S_{bc}, S_{ca}) = (1,0,0) \quad \text{or} \quad (0,1,0) \quad \text{or} \quad (0,0,1) \tag{4.2.34}$$

Due to both magnitudes being equal, then the proportion of negative sequence current with respect to the positive sequence is equal to one, i.e. $K_{in} = 1$. The phase shift of the negative sequence components with respect to the secondary-side voltage node, ϕ_{ivs}, is given as follows.

$$\phi_{ivs} = \begin{cases} \pi/3 & , \quad (S_{ab}, S_{bc}, S_{ca}) = (1,0,0) \\ -\pi & , \quad (S_{ab}, S_{bc}, S_{ca}) = (0,1,0) \\ -\pi/3 & , \quad (S_{ab}, S_{bc}, S_{ca}) = (0,0,1) \end{cases} \tag{4.2.35}$$

Although the secondary-side voltage is balanced, the negative sequence component of the current is generated due to the load unbalance. The previous equations assume that the phase shift of the positive sequence voltage is equal to zero. Nonetheless, it is shifted in $\pi/6$ rad with respect to the grid voltage, as Fig. 4.5 shows. Then, when transferring the negative sequence current to the MV side, an additional $\pi/6$ rad phase shift is added. Therefore $\phi_{in} = \phi_{ivs} + \pi/3$, and ϕ_{vin} is obtained as follows when considering that the negative sequence voltage of the grid is in phase with the positive sequence, i.e. $\phi_{vn} = 0$.

$$\phi_{vin} = \phi_{vn} - \phi_{in} = \begin{cases} -2\pi/3 & , \quad (S_{ab}, S_{bc}, S_{ca}) = (1,0,0) \\ 2\pi/3 & , \quad (S_{ab}, S_{bc}, S_{ca}) = (0,1,0) \\ 0 & , \quad (S_{ab}, S_{bc}, S_{ca}) = (0,0,1) \end{cases} \tag{4.2.36}$$

Therefore, according to (4.2.22), the CAPF due to balanced components will be the same for all load combinations. Nonetheless, because ϕ_{vin} changes for each scenario, the interaction between the negative sequence voltage and uncompensated unbalanced currents will generate additional additive or subtractive CAPF according to $\cos(\phi_{vin})$.

4.2.2 HDT efficiency

The CAPF increases as the efficiency of each element of the HDT decreases, reducing the overall efficiency of the HDT. Therefore, it is of interest to analyze how the efficiency of the HDT is affected by the operating conditions.

Once the CAPF is obtained in terms of the load and the equivalent parallel losses of the LFT, as shown in (4.2.22), the grid active power can be calculated according to the

following steps:

1. Based on (4.2.22), calculate the parallel converter current as $i_{p\alpha\beta} = \dfrac{P_p}{N_{sp}|V_n|}$.
2. Obtain the secondary-side current as $i_{s\alpha\beta} = i_{p\alpha\beta} + i_{L\alpha\beta}$.
3. Obtain the grid current as $i_{g\alpha\beta} = N_{sp} i_{s\alpha\beta} + i_{l\alpha\beta}$.
4. Calculate the average grid active power as $P_g = \text{mean}(v_{g\alpha\beta} \cdot i_{g\alpha\beta})$.
5. Calculate the HDT efficiency using $\eta_{HDT} = \dfrac{P_L}{P_g}$.

Following the previous steps, the efficiency of the HDT can be written as the following equation indicates.

$$\frac{1}{\eta_{HDT}} = \underbrace{\frac{1}{\eta_{HDTo}}}_{\substack{\text{Balanced} \\ \text{component}}} + \underbrace{K_n\left(1 - \frac{1}{\eta_{HDTo}\eta_{PC}}\right)}_{\substack{\text{Unbalanced} \\ \text{component}}} - \underbrace{\alpha_\eta}_{\substack{\text{Other} \\ \text{losses}}} \tag{4.2.37}$$

where the effect of the balanced components in the efficiency is represented by η_{HDTo}, which is observed for any grid conditions that result in $K_n = 0$, i.e., $K_{vn} = 0$, $K_{in} = 0$, or $\cos(\phi_{vin}) = 0$. The efficiency for balanced conditions is given as follows.

$$\eta_{HDTo} = \frac{1 - K'_{vp}}{1 - K_{vp}} \tag{4.2.38}$$

The effect of the negative sequence in the efficiency is only observed when $K_n \neq 0$. The latter occurs only when the series converter compensates for the unbalanced components of the grid voltage, and the parallel converter does not compensate for all the negative sequence components presented on the load voltage. Alternatively, this component can be written as follows.

$$K_n\left(1 - \frac{1}{\eta_{HDTo}\eta_{PC}}\right) = \frac{K_n}{\eta_{HDTo}(1 - K_{vp})}\left(1 - \frac{1}{\eta_{pc}\eta_{LFT}}\right) \tag{4.2.39}$$

In (4.2.37), the term α_η corrects the effect of the equivalent parallel losses of the LFT on the overall efficiency of the HDT. Two alternatives of the term α_η are shown below.

$$\alpha_\eta = \frac{1 - K_{vp} - \eta_{PC} + \eta_{PC}K'_{vp}}{\eta_{HDTo}\eta_{PC}}\frac{P_l}{P_L} = \frac{1 - \eta_{pc}\eta_{LFT}}{\eta_{pc}\eta_{LFT}\eta_{HDTo}}\frac{P_l}{P_L} \tag{4.2.40}$$

By inspecting (4.2.22) and (4.2.37) under balanced conditions, it can be expected that the efficiency of the HDT decreases under voltage sags. This occurs due to the additive

CAPF will increase the losses on the different components of the HDT. The opposite is expected under a voltage swell. Although there will be losses in the power converter stage, the subtractive CAPF reduces the voltage drop through the LFT, increasing the efficiency of the LFT and consequently improving the efficiency of the HDT.

Comments on the ideal operation of the HDT

Based on (4.2.37) and (4.2.38), if the efficiency of the LFT and power converters are 100%, the efficiency of the HDT is 100% as well. Therefore, all the active power supplied by the series converter during the compensation of a voltage sag/swell is provided by the parallel converter, generating the CAPF phenomenon. In this scenario, the additional CAPF is not transferred to the grid side. Then, the grid just supplies the load.

4.3 Oscillatory power flow and DC-Link ripple

The unbalances presented on the grid, HDT, and load operation will generate an Oscillatory Power Flow (OPF) that will generate oscillations in the DC-Link voltage.

This section models the DC-Link voltage ripple and the OPF, considering the impact of the CAPF on them.

4.3.1 DC-Link ripple model

Based on (2.3.17), the following equation models the DC-Link, taking as a reference the simplified model of Fig. 4.2.

$$\frac{C_{dc}}{2}\frac{\mathrm{d}v_{dc}^2}{\mathrm{d}t} = \underbrace{v_{s\alpha\beta}\cdot i_{p\alpha\beta}}_{p_p} \quad - \quad \underbrace{v_{se\alpha\beta}\cdot i_{g\alpha\beta}}_{p_{se}} \tag{4.3.1}$$

Considering an unbalanced and steady-state operation and that both active power are decomposed according to (4.2.1), the following DC-Link voltage equation is obtained.

$$\frac{C_{dc}}{2}\frac{dv_{dc}^2}{dt} = \underbrace{(P_p - P_{se})}_{\approx 0 \text{ in steady state}} + \underbrace{(\widetilde{p}_p - \widetilde{p}_{se})}_{\Delta\widetilde{p}} \tag{4.3.2}$$

In order to have a stabilized DC-Link voltage, the parallel converter must provide the average active power demanded by the series converter in addition to compensating the system losses. On the other side, the difference of the oscillatory components, $\Delta\widetilde{p}$, is highly dependent on the grid, HDT, and load operating conditions. The value of $\Delta\widetilde{p}$ can be considered nonzero for most unbalanced operating conditions unless particular

conditions are met. The equivalent circuital model of the DC-Link is shown in Fig. 4.2(c). The steady-state relationship between the squared capacitor voltage and the oscillatory components of the active power is given as follows.

$$v_{dc}^2 = \frac{2}{C_{dc}} \int \Delta\widetilde{p} \mathrm{d}t + V_{dc}^2 \tag{4.3.3}$$

where V_{dc}^2 is the average steady-state DC-Link voltage. When operating in unbalanced conditions, the oscillatory component corresponds to a second-order harmonic, whose general amplitude and phase are $|\Delta\widetilde{p}|$ and ϕ_p, respectively.

$$\Delta\widetilde{p} = |\Delta\widetilde{p}| \cos(2\omega t + \phi_p) \tag{4.3.4}$$

Then, by applying the Fourier Transform and considering the conditions previously mentioned, the steady-state squared voltage can be written according to the following equation.

$$v_{dc}^2 = V_{dc}^2 + \frac{|\Delta\widetilde{p}|}{\omega C_{dc}} \cos(2\omega t + \phi_p - \pi/2) \tag{4.3.5}$$

The maximum and minimum squared voltages are presented as follows.

$$\begin{bmatrix} v_{dcmax}^2 \\ v_{dcmin}^2 \end{bmatrix} = \begin{bmatrix} V_{dc}^2 + \dfrac{|\Delta\widetilde{p}|}{\omega C_{dc}} \\ V_{dc}^2 - \dfrac{|\Delta\widetilde{p}|}{\omega C_{dc}} \end{bmatrix} \tag{4.3.6}$$

Then, the maximum and minimum DC-Link voltages are calculated.

$$\begin{bmatrix} v_{dcmax} \\ v_{dcmin} \end{bmatrix} = \begin{bmatrix} \sqrt{V_{dc}^2 + \dfrac{|\Delta\widetilde{p}|}{\omega C_{dc}}} \\ \sqrt{V_{dc}^2 - \dfrac{|\Delta\widetilde{p}|}{\omega C_{dc}}} \end{bmatrix} \tag{4.3.7}$$

The exact equation that models the capacitor voltage ripple, Δv_{dc}, in terms of the oscillating active power is expressed as follows.

$$\Delta v_{dc} = \sqrt{V_{dc}^2 + \frac{|\Delta\widetilde{p}|}{\omega C_{dc}}} - \sqrt{V_{dc}^2 - \frac{|\Delta\widetilde{p}|}{\omega C_{dc}}} \tag{4.3.8}$$

The previous equation can be simplified as shown below when the oscillating active power does not generate abnormal DC-Link oscillations.

$$\Delta v_{dc} = \frac{1}{\omega C_{dc} V_{dc}} |\Delta \widetilde{p}|, \quad \text{when } V_{dc}^2 \gg \frac{|\Delta \widetilde{p}|}{\omega C_{dc}} \tag{4.3.9}$$

Using (4.3.8) and (4.3.9), the ripple of the DC-Link can be estimated and studied for different grid conditions.

4.3.2 Oscillatory power flow model

This section models the OPF, considering the efficiency of the power converters and LFT. Nonetheless, the terms associated with the series impedance and parallel losses of the transformer are neglected in order to simplify the mathematical expressions. This simplification is done because the values of OPF applied to the DC-Link ripple model are then filtered by the DC-Link system. Additionally, the simplified model of Fig. 4.2, considers the series and parallel power converters as ideal controlled voltage and current sources. The internals, such as unbalances on the CTs, output capacitors, and reactances are neglected. Therefore, even if the efficiency values and internal impedance of the LFT were taken into consideration, the obtained OPF would deviate from the real values due to the simplification of the power converter models. Thus, a simplified approach is taken to have a grasp of the OPF behavior, which is good enough for the DC-Link ripple analysis.

In a similar fashion as in the previous section, the oscillatory components of the active power of the series converter are obtained from (4.2.14) and (4.2.15) neglecting the terms associated with R_{LFT} and L_{LFT}.

$$\begin{aligned} \widetilde{p}_{se} \approx & \underbrace{K_{vp}(1-T_{in})K_{in}P_L\cos(\theta_{in})}_{\substack{\text{Unbalanced} \\ \text{load component}}} - \underbrace{K_{vn}(1-T_{iq})K_{iq}P_L\sin(\theta_{vn})}_{\substack{\text{Unbalanced grid voltage} \\ \text{and reactive load}}} \\ & - \underbrace{\frac{1-K'_n}{1-K'_{vp}}K_{vn}P_L\cos(\theta_{vn})}_{\substack{\text{Unbalanced} \\ \text{grid and load component}}} + \underbrace{\frac{1-\eta_{PC}\eta_{HDTo}}{\eta_{PC}\eta_{HDTo}}K_{vn}P_l\cos(\theta_{vn})}_{\substack{\text{Other losses} \\ \text{component}}} \end{aligned} \tag{4.3.10}$$

On the other hand, the oscillatory components for the active power of the parallel converter are given by the product of the secondary side voltage and the injected negative sequence. This is the only condition in which the instantaneous active power of the parallel converter has an oscillatory component, which is given below.

$$\widetilde{p}_p = -\underbrace{T_{in}K_{in}P_L\cos(\theta_{in})}_{\substack{\text{Unbalanced}\\ \text{load component}}} \tag{4.3.11}$$

The DC-Link controller regulates the average value of the DC voltage, and the oscillatory power components of both converters are not regulated. Therefore, they will generate oscillations on the DC-Link voltage according to the amplitude of $\Delta\widetilde{p} = \widetilde{p}_p - \widetilde{p}_{se}$, which can be written as follows.

$$\Delta\widetilde{p} = \Delta\widetilde{p}_{ug} + \Delta\widetilde{p}_{ul} + \Delta\widetilde{p}_{ugl} + \Delta\widetilde{p}_{ll} \tag{4.3.12}$$

where $\Delta\widetilde{p}_{ug}$ contains the effect of the grid voltage unbalance, $\Delta\widetilde{p}_{ul}$ the load unbalance, $\Delta\widetilde{p}_{ugl}$ the interaction of both grid and load unbalance, and $\Delta\widetilde{p}_{ll}$ contains the effect of the additional losses of the transformer. They are given by the following equations.

$$\Delta\widetilde{p} = \begin{cases} \Delta\widetilde{p}_{ug} + \Delta\widetilde{p}_{ll}, & \text{for unbalanced grid voltage} \\ \Delta\widetilde{p}_{ul} + \Delta\widetilde{p}_{ll}, & \text{for unbalanced load} \\ \Delta\widetilde{p}_{ug} + \Delta\widetilde{p}_{ul} + \Delta\widetilde{p}_{ugl} + \Delta\widetilde{p}_{ll}, & \text{for unbalanced grid and load} \end{cases} \tag{4.3.13}$$

The expressions for $\Delta\widetilde{p}_{ug}$, $\Delta\widetilde{p}_{ul}$, $\Delta\widetilde{p}_{ugl}$, and $+\ \Delta\widetilde{p}_{ll}$ are given as follows.

$$\Delta\widetilde{p}_{ug} = \underbrace{\frac{K_{vn}}{1-K'_{vp}}P_L\cos(\theta_{vn})}_{①} \quad + \quad \underbrace{K_{vn}K_{iq}(1-T_{iq})P_L\sin(\theta_{vn})}_{②} \tag{4.3.14a}$$

$$\Delta\widetilde{p}_{ul} = -(T_{in} - T_{in}K_{vp} + K_{vp})K_{in}P_L\cos(\theta_{in}) \tag{4.3.14b}$$

$$\Delta\widetilde{p}_{ugl} = -\frac{K'_n}{1-K'_{vp}}K_{vn}P_L\cos(\theta_{vn}) \tag{4.3.14c}$$

$$\Delta\widetilde{p}_{ll} = -\frac{1-\eta_{PC}\eta_{HDTo}}{\eta_{PC}\eta_{HDTo}}K_{vn}P_l\cos(\theta_{vn}) \tag{4.3.14d}$$

As it is expected, the OPF depends on the amount of negative sequence voltage injected by the power converter. Additionally, it can be seen that in some scenarios the CAPF reinforces the OPF, which, depending on their magnitude and phase relation of

the unbalances, could negatively affect the DC-Link voltage. Fig. 4.4 exemplifies the OPF for different grid and load conditions.

Unbalanced grid operation

Following (4.3.14a), the active power oscillation has two distinct components:

1. The first term is given by the following equation.

$$\textcircled{1} = \frac{K_{vn}}{1 - K'_{vp}} P_L \cos(\theta_{vn}) \tag{4.3.15}$$

   In this scenario, the OPF appears due to the interaction between the active load with the positive and negative sequence components of the grid voltage disturbance. It can be that this term is affected by the CAPF due to the presence of the term $1 - K'_{vp}$ in the denominator. Therefore, during compensations of positive sequence voltage disturbances, such as voltage sags or swells, the OPF will have a nonlinear behavior.

2. The OPF due to reactive currents is given by:

$$\textcircled{2} = K_{vn} K_{iq} (1 - T_{iq}) P_L \sin(\theta_{vn}) \tag{4.3.16}$$

   This expression corresponds to the interaction between the injected negative sequence voltage and the uncompensated reactive currents of the load. It can be seen that when $T_q = 1$, i.e., the parallel converter compensates all the reactive load, achieving unit PF, no reactive currents circulate through the series converter. Therefore, no OPF occurs in this case. The OPF decreases linearly with the reactive current compensation. Also, there is no interaction between the reactive currents and the CAPF.

When operating under the conditions of an unbalanced grid voltage but a balanced load, it is possible to obtain the maximum OPF as follows.

$$|\Delta \widetilde{p}_{ug}| = \left| \frac{K_{vn} P_L}{1 - K_{vp}} \right| \sqrt{1 + (1 - K_{vp})^2 (1 - T_q)^2 K_q^2} \tag{4.3.17}$$

Unbalanced load operation

On the other hand, the maximum OPF for a balanced grid voltage but an unbalanced load is given by the next equation.

$$|\Delta\widetilde{P}_{ul}| = |T_{in} + K_{vp} - K_{vp}T_{in}|\,|K_{in}||\overline{P}_L| \tag{4.3.18}$$

In this case, the OPF depends on the interaction between the positive sequence voltage injected by the series converter and the uncompensated unbalanced currents of the load, as well as the effect of power oscillation due to the injection of negative sequence currents by the parallel converter.

Unbalanced grid and load operation

The maximum OPF when both grid and load are unbalanced is obtained based on (4.3.12). Obtaining a simplified expression is cumbersome, therefore a conservative expression is obtained based on the triangular inequality.

$$|\Delta\widetilde{p}| \leq |\Delta\widetilde{p}_{ug}| + |\Delta\widetilde{p}_{ul}| + |\Delta\widetilde{p}_{ugl}| + |\Delta\widetilde{p}_{ll}| \tag{4.3.19}$$

Then, the maximum magnitude of the OPF is obtained by adding the OPF of the different operating conditions, i.e., by adding the maximum OPF given by the unbalanced grid operation, unbalanced load operation, and unbalanced grid and load operation.

4.3.3 DC-Link design

The DC-Link ripple is presented in (4.3.8), and it depends on the magnitude of the OPF, which at the same time depends on the operating conditions of the HDT. Therefore, the equation shown in (4.3.19) can be utilized to estimate the OPF for the worst-case operation scenario. Then, from (4.3.8), the minimum DC-Link capacitance to sustain the operation of the HDT can be obtained using the following equation.

$$C_{dc_{min}} \geq \frac{2|\Delta\widetilde{p}|_{max}}{\omega|\Delta v_{dc}|_{min}\sqrt{4V_{dc}^2 - |\Delta v_{dc}|_{min}^2}} \tag{4.3.20}$$

Fig. 4.6 shows the dependence of the minimum DC-Link capacitance with the injected positive voltage (K_{vp}) when $K_{vn} = 0.1$ for different DC-Link ripples. Due to the effect of the CAPF, a higher DC-Link capacitance is required when the balanced voltage sag increases.

4.4 Methods to reduce the CAPF

In the previous section, it was shown that the CAPF negatively impacts the efficiency of the HDT, as it increases the amount of power that the LFT and power converters process and increases the equivalent series voltage drop to be compensated. Therefore, two methods to reduce the CAPF are presented in this section. The first one is based on modifying the control strategy of the series converter by injecting reactive power. In the second method, the structure of the HDT is modified by adding a BESS connected to the DC-Link. Both alternatives and their advantages and disadvantages are presented in the following sections.

4.4.1 Reactive power injection

The analysis shown in the previous sections considers that the voltage injected by the series converter is in phase with the grid voltage. Nonetheless, it is possible to force the converter to inject reactive power exclusively to regulate the grid voltage [89].

Only the series converter is of concern. Therefore, the circuit is simplified to the representation shown in Fig. 4.7. The circuit is composed of the grid voltage, the injected series voltage, and a controlled current source that models the grid current. The voltage on the current source terminals corresponds to the voltage of the MV side of the main LFT. The objective of this section is to show that by a proper voltage injection, the CAPF can be reduced. Therefore, the simplified model neglects the losses of the LFT and power converter stages and only considers the balanced components of the grid voltage and load.

Considering that in order to inject reactive power, the injected series voltage must be in quadrature with the grid current. Fig. 4.8(a)–(c) shows different output operating vectors considering different load PF. It can be seen that as the PF increases, the series voltage magnitude required to regulate the secondary side voltage increases.

The following equation relates the positive sequence voltage phasors of the grid, series converter, and MV side of the LFT under the conditions described previously. For ease of representation, the reference node is set on the primary-side terminals of the LFT.

$$\underbrace{(1-K_{vp})\cancel{|V_n|}\angle\phi_{gvp}}_{\text{Grid voltage}} + \underbrace{K_{se}\cancel{|V_n|}\angle(\phi_{gip}\pm\pi/2)}_{\text{Series voltage}} = \underbrace{\cancel{|V_n|}\angle 0°}_{\text{Primary voltage}} \tag{4.4.1}$$

where ϕ_{gvp} and ϕ_{gip} correspond to the grid and current phase shift with respect to the load voltage, and K_{se} models the proportion of the series injected voltage with respect to

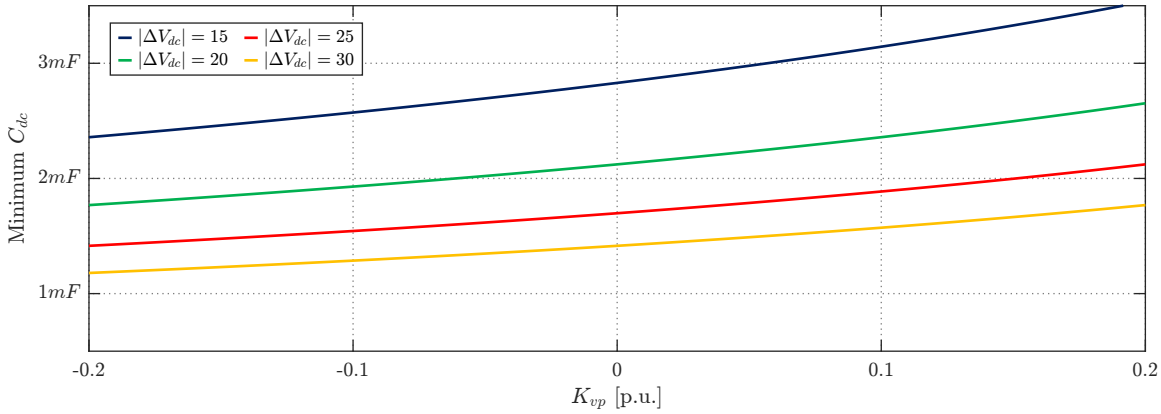


Fig. 4.6. Minimum DC-Link capacitance for $K_{vn} = 0.1$ and $K_{vp} = [-0.2, 0.2]$ for a different minimum DC-Link ripples.

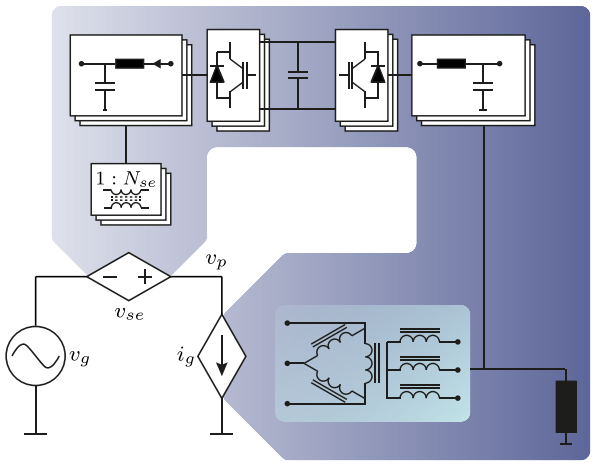


Fig. 4.7. Reactive power compensation - Reference circuit

the nominal grid voltage. Due to the reference node being the primary of the LFT, and its phase-shift being equal to zero, the phase-shift of the grid current is a direct measure of the PF.

$$PF_p = \cos(\phi_{gip}) \tag{4.4.2}$$

After simplification, the previous equation can be written in terms of the following hyperbola.

$$\underbrace{(1 - K_{vp})^2}_{|V_g|^2_{p.u.}} - (K_{se} \pm \sin(\phi_{gip}))^2 = \cos(\phi_{gip})^2 \tag{4.4.3}$$

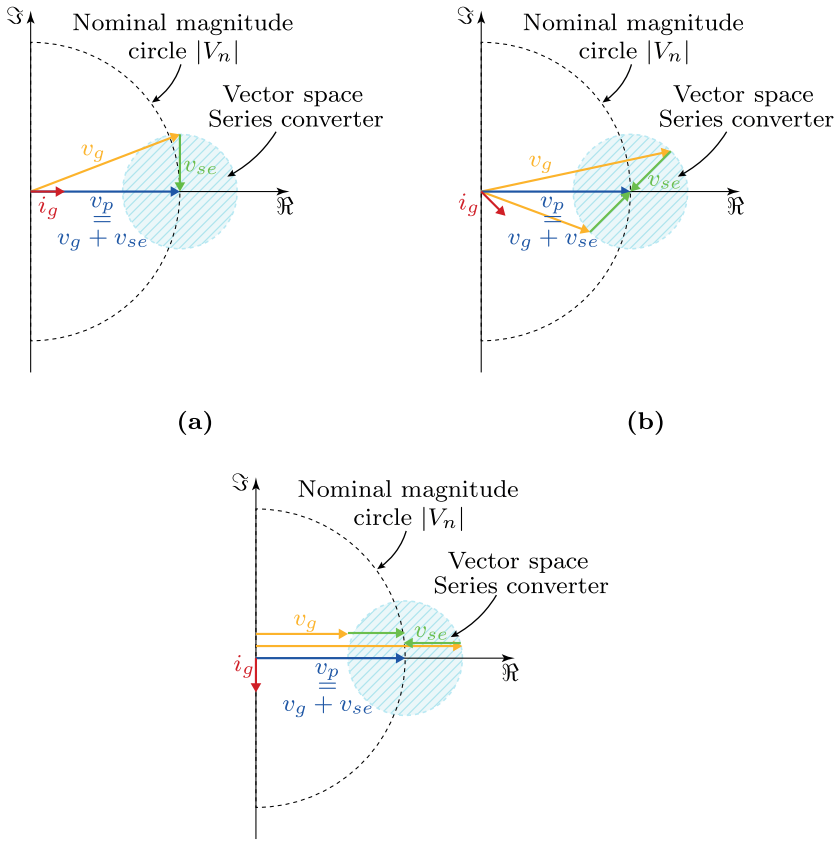


Fig. 4.8. Reactive power injection mode - Operating vectors for different load PF. **(a)**. PF = 1. **(b)** PF $\leq$ 1. **(c)** PF = 0.

Based on the previous equation, the relation between the series voltage and the grid voltage, when the load voltage is regulated to its rated value, is shown in Fig. 4.9(a). There are two limits to consider when injecting reactive power. The first limit corresponds to the maximum series voltage available, which in Fig. 4.9(a) is given by the intersection between the operation curves and the line representing the maximum series voltage available, $\pm\hat{K}_{se}$. The second limit corresponds to the maximum voltage that is mathematically possible to be injected, corresponding to the vertices of the hyperbola. The vertices and the intercept with the maximum series voltage are given below.

$$\left(|V_g|^v_{p.u.},\ \ K^v_{se}\right) = \left(\cos(\phi_{gip}),\ \ \pm\sin(\phi_{gip})\right) \tag{4.4.4a}$$

$$\left(|\hat{V}_g|_{p.u.},\ \ \hat{K}_{se}\right) = \left(\sqrt{1+\hat{K}^2_{se} \pm 2\hat{K}_{se}\sin\phi_{gip}},\ \ \pm\hat{K}_{se}\right) \tag{4.4.4b}$$

If the PF is continuously changed, then Fig. 4.9(b) shows the allowed grid voltage region with respect to the current angle. In this case a 0.5 p.u. series converter is utilized for visualization purposes. If the disturbed grid voltage magnitude falls inside the operating region, the HDT can regulate the load voltage to its rated value. Although it is possible to utilize reactive power for voltage compensation, the regulation capabilities of the HDT are reduced. For high PF, the HDT can only regulate voltage swells, requiring high actuation voltages. Nonetheless, the HDT can compensate for both swells and sags as the PF decreases. Alternatively, the load voltage can be regulated between an admissible band, which would extend the operating region presented in Fig. 4.9(b). Nonetheless, it

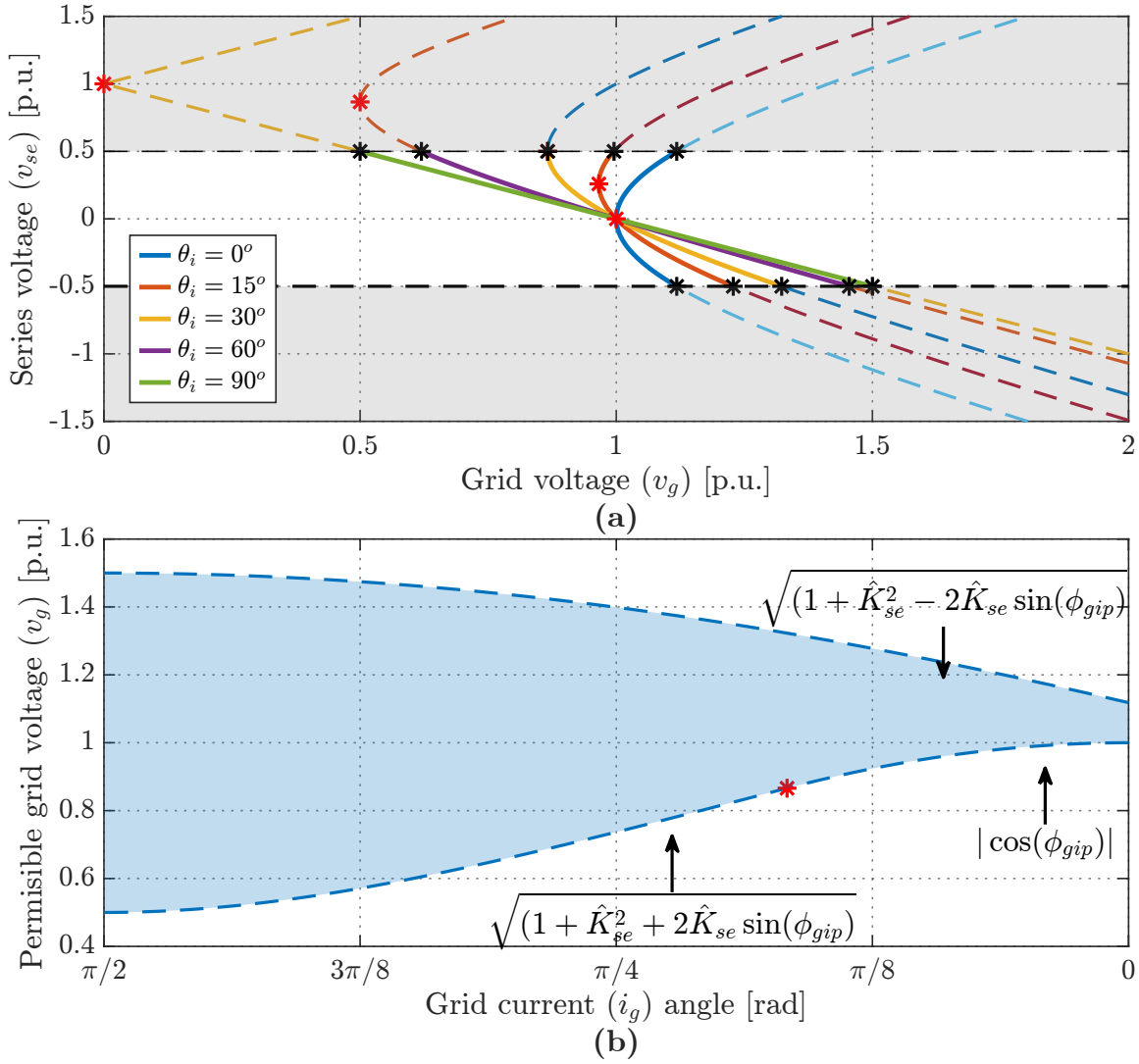


Fig. 4.9. Operating region when using reactive power compensation where the maximum series voltage is 0.5 p.u. **(a)**. I-IV quadrant of the series voltage vs. grid voltage for different PFs. **(b)** Permissible grid voltages vs. load PF.

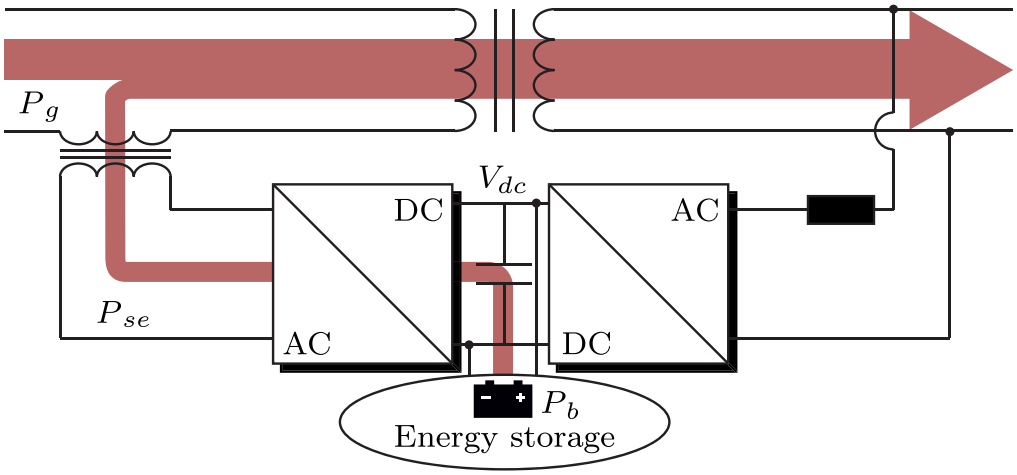


Fig. 4.10. Power flow of an HDT connected to a BESS.

is out of the scope of this work.

If the series power converter works in the operating regions shown in Fig. 4.9, then no active power will be injected on its output terminals. Nonetheless, there is a demand for active power from the DC-Link due to the power converter losses. Therefore, in order to regulate the DC-Link voltage, the parallel converter just compensates for the losses of both power converters.

4.4.2 Power routing using the DC port

By integrating a BESS into the HDT, as shown in Fig. 4.10, the series converter can extract energy from the DC system in order to supply the voltage disturbances. The CAPF is broken by not utilizing the parallel converter to balance the DC-Link energy.

Considering the BESS is connected to the DC-Link, and forcing P_p to zero, implies that the BESS must supply the active power required by the series converter in order to balance the DC-Link energy. Considering the additional losses of the transformer, its efficiency, the efficiency of the BESS power converters, and an operation with balanced and unbalanced components, the following expression for the average active power of the BESS is obtained.

$$P_b = \frac{1-\eta_{LFT}+\eta_{LFT}K_{vp}}{\eta_{SEB}\eta_{LFT}}P_L - \frac{K_{vn}K_{in}(1-T_{in})\cos(\phi_{vin})}{\eta_{SEB}}P_L - \frac{1-K_{vp}}{\eta_{SEB}}P_l \qquad (4.4.5)$$

where η_{SEB} is the efficiency from the BESS to the output of the series converter stage. Unlike the previous CAPF results, when integrating a BESS, the active power of the

series converter is simply proportional to the total series disturbance, i.e., the grid voltage sag/swell plus the series voltage drop of the LFT. The terms K'_{vp}, K'_n do not appear, and the division by $(1 - K'_{vp})$ is not present, reducing the power required by the BESS and avoiding the CAPF.

By mitigating the CAPF, the amount of power processed by the LFT decreases, as well as the power processed by the series converter. On the other side, a lower current magnitude is translated into a lower voltage drop on the LFT and CTs, and therefore the required compensation voltage of the series converter is reduced, improving the utilization of the power converters.

4.5 Control of the HDT for CAPF analysis

The HDT controller shown in Fig. 4.11 is used to study the CAPF. It includes the capacitor voltage controller of the series converter, the DC-Link, and the internal current controller of the parallel converter. The load current decomposition filter is included in Fig. 4.12.

4.5.1 Series converter controller

The controller of the series converter consists of the capacitor voltage regulator shown Fig. 4.11(a). A resonant controller is utilized to provide tracking for positive and negative sequence voltages.

$$C_{v1}(s) = \frac{K_{vr1}s^2 + K_{vr2}s + K_{vr3}}{s^2 + \omega^2} \tag{4.5.1}$$

The inductor current is multiplied by K_i and added directly to the output voltage in order to provide active damping and improve stability.

An external load voltage magnitude controller is utilized, which preserves the positive sequence of the grid voltage. Alternatively, the voltage magnitude controller used during reactive power compensation is shown.

4.5.2 Parallel converter controller

The controller of the parallel converter is shown in Fig. 4.11(b). The internal controller regulates the output converter current, i_p. A resonant controller such as (4.5.1) is utilized, whose parameters are K_{ir1}, K_{ir2}, and K_{ir3}. The feedforward terms correspond to the capacitor voltage and secondary side current, which act as active damping terms. Both

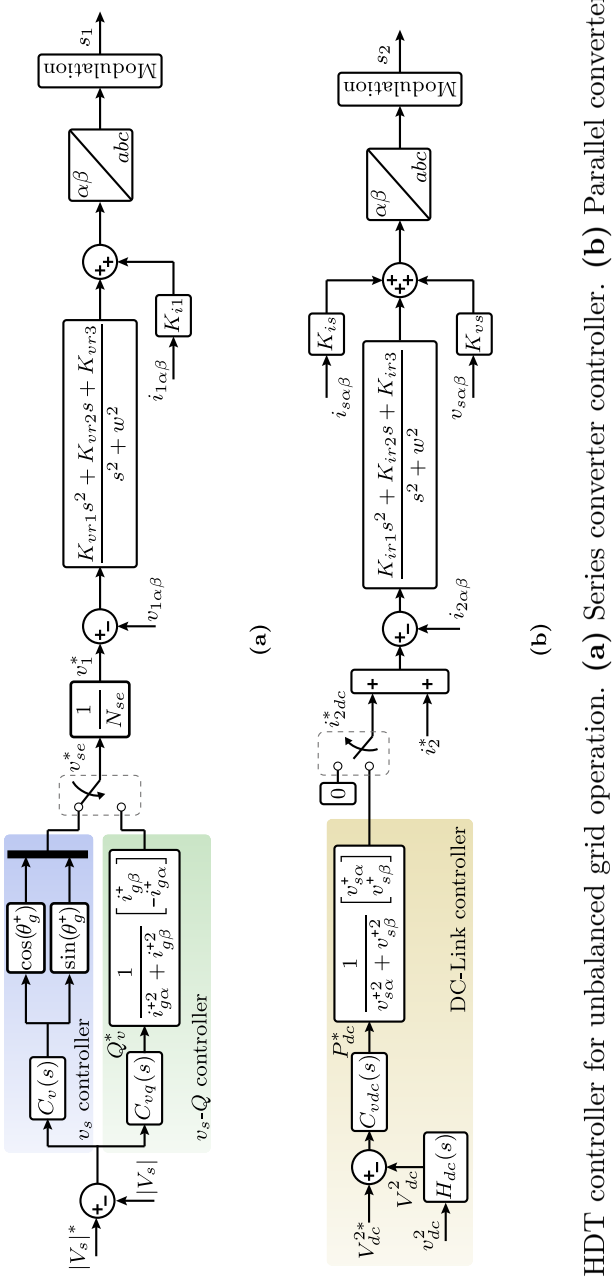


Fig. 4.11. HDT controller for unbalanced grid operation. **(a)** Series converter controller. **(b)** Parallel converter controller.

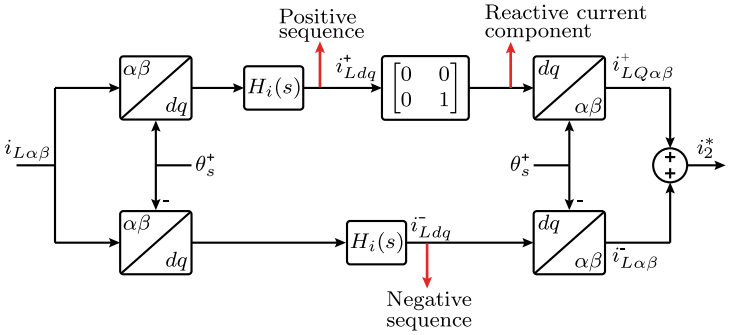


Fig. 4.12. Load current filter for CAPF analysis.

variables are multiplied by K_{vs}, and K_{is}, respectively. This controller can be designed based on the LQR method [92].

The double grid frequency oscillation component is removed from the capacitor energy using a low-pass filter and a notch filter tuned to the second harmonic with the following generalized transfer function.

$$H_{dc}(s) = \frac{n_{dc1}s^2 + n_{dc2}s + n_{dc3}}{s^3 + d_{dc1}s^2 + d_{dc2}s + d_{dc3}} \tag{4.5.2}$$

The DC-Link voltage is regulated using a conventional PI controller, $C_{vdc}(s)$, which gives the active power reference of the parallel converter. The current reference is obtained using the Instant Power Theory (IPT) with positive sequence voltages. The proportional and integral gains of the DC-Link controller are K_{pdc} and K_{idc}, respectively.

4.5.3 Load current filtering

The diagram presented in Fig. 4.12 corresponds to the current reference generator of the parallel converter.

The load currents are rotated using the positive and negative sequences of the load voltage. Their oscillatory components are eliminated using the filter H_i, which is similar to (4.5.2). Its parameters are given by n_{i1}, n_{i2}, n_{i3}, d_{i1}, d_{i2}, and d_{i3}.

Additionally, to obtain the reactive current, the d component of the positive sequence is set to zero. Finally, both currents are rotated back to the $\alpha\beta$ reference frame.

4.6 Simulation results

Fig. 4.13 shows the results of the HDT under different operation conditions. Initially, the HDT is connected to a balanced grid voltage and load. Then, at $t = 80$ms, a 10% grid voltage sag is applied, generating a CAPF of 5847W, which roughly corresponds to 11.69% of the average load active power. Taking into consideration the system losses, the CAPF coincides with (4.2.26) when $K_{vp} = 0.1$, giving a theoretical ideal CAPF of 11.1%. Next, at $t = 200$ms, the grid voltage becomes unbalanced, with $K_{vn} = 0.1$. The disturbance is regulated by the series converter, which according to the theoretical analysis, does not influence the CAPF. Nonetheless, an OPF exists, which causes a voltage ripple of 15.8V on the DC-Link. A similar value of 15.6V is obtained for the theoretical ripple, calculated using (4.3.12) and (4.3.8).

At $t = 350$ms, an unbalanced load is connected, and the negative sequence compensation of the parallel converter is turned off, i.e., $T_{in} = 0$. The results show that the CAPF increases. This is in accordance with the ideal CAPF equation of (4.2.27) for the grid and uncompensated load unbalances. In this scenario, the theoretical CAPF corresponds increases to 10.4 kW. This is marginally lower than the CAPF shown in Fig. 4.13(g), which corresponds to 10.5 kW when the losses are taken into consideration. On the other hand, the measured and theoretical capacitor ripples are 28.9V and 30V.

Finally, at $t = 440$ms, the parallel converter compensates the load unbalanced by setting $T_{in} = 1$. According to (4.2.27), no additional CAPF is generated due to the negative sequence of the load current does not flow through the series converter. Considering the total average active power and $K_{vp} = 0.1$, the theoretical CAPF corresponds to 8.78kW. The CAPF shown in the results corresponds to 9.18kW. The difference corresponds to the power converter losses, which in this case increase due to the increment in the current when the power converter compensates for the unbalanced load, as Fig. 4.13(f) shows. The theoretical and actual CAPF correspond to 11.1% and 11.6%, respectively. Due to the high amplitude negative sequence currents, the OPF generates a measured and theoretical capacitor ripple of 97.9V and 96.7V, respectively.

4.7 Experimental results

This section presents the experimental results of the CAPF analysis. The diagrams of the experimental setup for each test are presented in the **Appendix B**. Fig. B.2 shows the experimental setup for the CAPF and efficiency analysis, whereas Fig. B.3 shows the experimental setup for the HDT operating under unbalanced conditions. The same setup

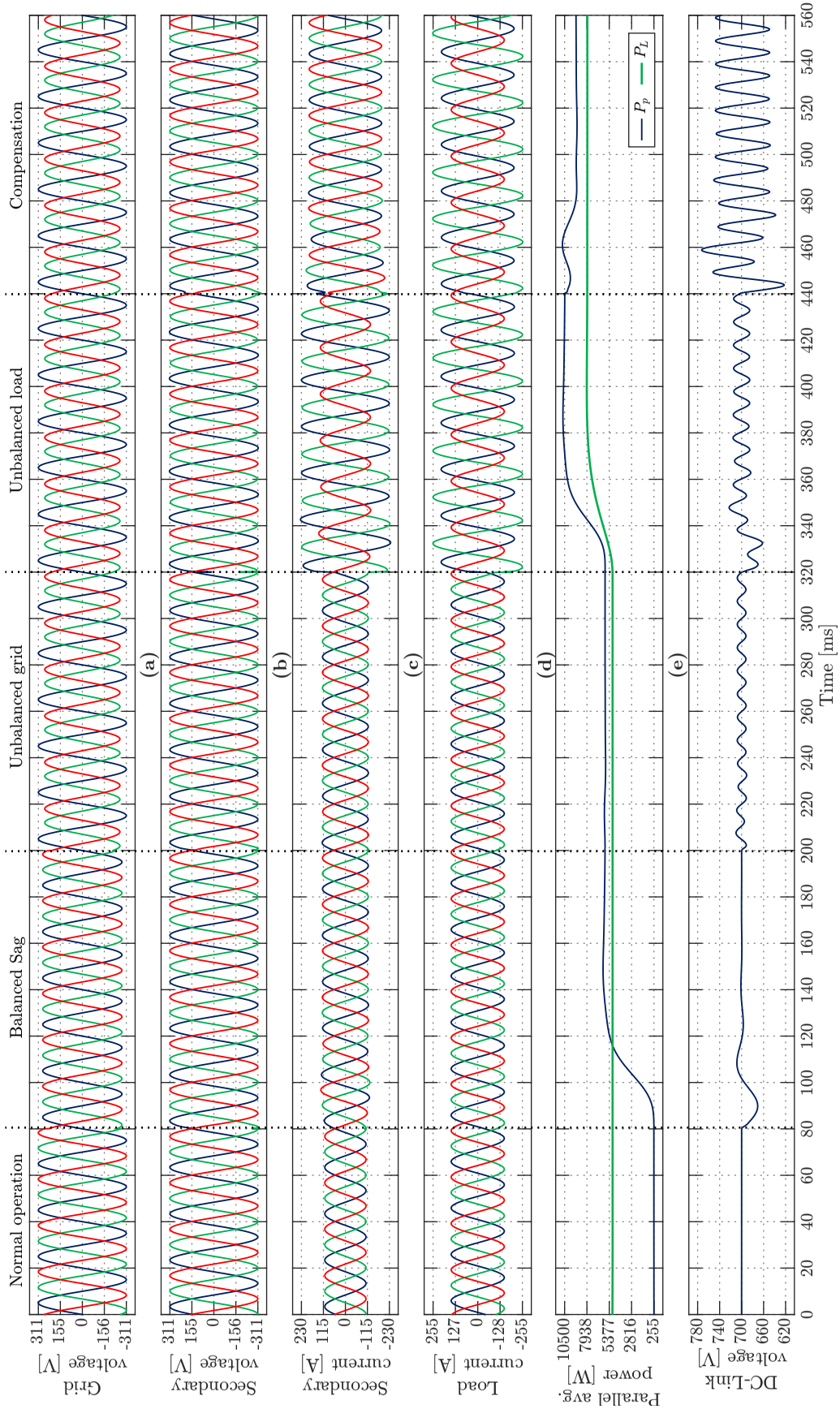


Fig. 4.13. Simulation results - Dynamic response of the HDT. **(a)** Grid voltage. **(b)** Secondary-side voltage. **(c)** Secondary-side current. **(d)** Load current. **(e)** CAPF and average load power. **(f)** DC-Link voltage.

is employed when the reactive power injection method is tested.

The system and control parameters are listed in Table 4.1. The efficiency results are obtained utilizing CTs with a turns ratio of 1/10 in order to provide a maximum voltage compensation of ±10%. Then, in the remaining experimental results, CTs with a turns ratio of 1/5 are utilized to extend the compensation up to ±20% and increase the CAPF in order to prove the CAPF reduction methods.

Remark: The experimental results which were included in the derived publication of this chapter were obtained using two oscilloscopes Tektronix MSO58B and MDO34. These results correspond to the Fig. 4.14, Fig. 4.15, Fig. 4.17, and Fig. 4.18.

Due to the channel number limitation of the oscilloscope, the remaining experimental result shown in Fig. 4.16 was obtained directly from the microcontroller of both power converters and measurement board. Thus, due to memory restrictions, these results were obtained using an equivalent sampling time of 160μs.

It is worth mentioning that due to the configuration of the control platform, the load current is not measured directly. Instead, the summation of the load current with the capacitor current is shown. On the other side, the load current is directly measured in the results obtained via the oscilloscopes.

Table 4.1. HDT and control parameters for CAPF analysis.

HDT parameters					
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**
$\|v_g\|$	100V	$\|v_s\|$	100V	ω	$2\pi 50$
V_{dc}	350V	C_{dc}	6400μF	L_s	500μH
C_1 C_2	12.6μF	L_1 L_2	200μH	N_{se}	1/10 - 1/5
Control parameters					
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**
K_{i1}	16.35	K_{vr1}	0.05	K_{vr2}	38.6
K_{vr3}	1.5e4	K_{pvq}	0	K_{ivq}	500
K_{ir1}	0.91	K_{ir2}	1.7e3	K_{ir3}	1.3e6
K_{is}	1.94	K_{vs}	-0.29	K_{pdc}	0.09
K_{idc}	0.4	K_{pvs}	0	K_{ivs}	40
n_{dc1},n_{i1}	1000	n_{dc2},n_{i2}	888.57	n_{dc3},n_{i3}	3.94e8
d_{dc1},d_{i1}	3.63e3	d_{dc2},d_{i2}	1.49e6	d_{dc3},d_{i3}	3.94e8

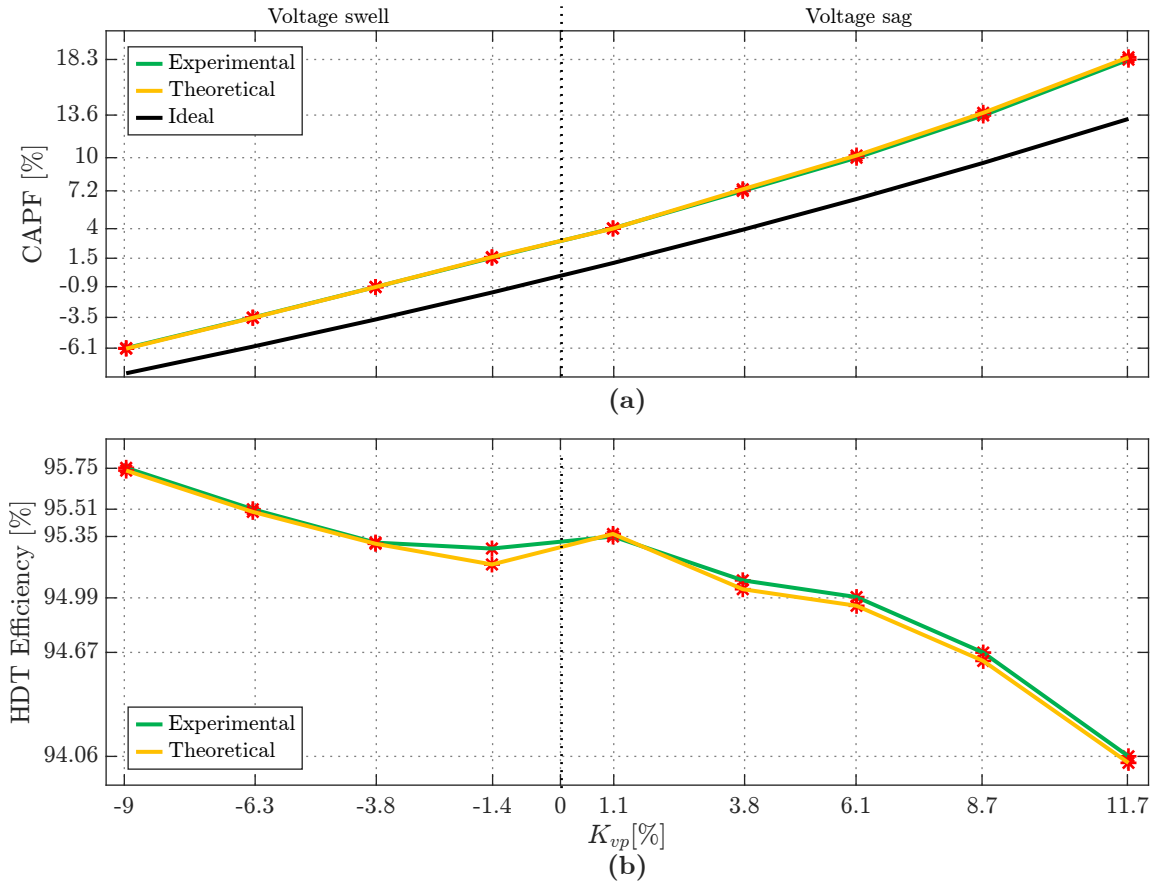


Fig. 4.14. Experimental versus theoretical CAPF and efficiency with respect to the grid voltage sag/swell. **(a)** CAPF. **(b)** HDT efficiency.

4.7.1 CAPF and efficiency of the HDT

The results in Fig. 4.14 show the nonlinear relation between the CAPF and the HDT efficiency with the magnitude of the voltage sag/swell. When the voltage sag increases, a higher percentage of CAPF is required to regulate the load voltage, incrementing the current magnitude through the LFT. Contrarily, a subtractive CAPF is generated during voltage swells. Compared to the ideal CAPF, it can be seen that when the losses are considered, the CAPF curve is shifted up in the y-axis, and the steepness of the curve increases for higher values of K_{vp}.

Based on the values of the sag/swell magnitude and LFT and power converter efficiency, which are measured for every operation point, the theoretical values obtained using (4.2.22) and (4.2.37). The theoretical values match the experimental measurements. The value of P_l is obtained experimentally, being equal to 31.6W.

4.7.2 Balanced and unbalanced operation

Fig. 4.15 shows the results of the HDT under different operation conditions. In Fig. 4.15(a), the HDT operates as an LFT supplying a load with a nominal power of 3kW. Then, in Fig. 4.15(b), the power converters are turned on, and the secondary side voltage is regulated to its rated value. During this operation, the parallel converter consumes 385W. A balanced voltage sag of 15% is applied in Fig. 4.15(c), for which a CAPF of 1331W is obtained, corresponding to 44% of the nominal power. Next, Fig. 4.15(d) shows that a 10% of negative sequence voltage is added to the grid. As expected, no additional CAPF is generated. Nonetheless, when unbalanced currents are consumed by the load and the parallel converter provides no compensation, as Fig. 4.15(e) shows, the CAPF increments to 1473W due to the interaction between the negative sequence voltage and current on the series converter. The phase shift of the negative sequences corresponds to π to achieve the maximum additional CAPF. Finally, in Fig. 4.15(f), the parallel converter balances the load, which decreases the CAPF to its previous value according to (4.2.22), due to there is no negative sequence interaction on the series converter.

Negative sequences interaction

Fig. 4.16 show the experimental results of the example presented previously in the example of Fig. 4.5. Three different cases are studied, connecting the same resistive load between the phases a-b, then b-c, and finally c-a. For all scenarios, the following grid voltage of Table 4.2 is employed, which is equivalent to applying a balanced sag of 10%, with a negative sequence component of 10% with phase-shift equal to 0°. The grid voltages shown in Fig. 4.16 differ because they correspond to the line voltage, considering also the line voltage drops. On the other side, as explained in the example, the active power for each scenario is the same, but the equivalent phase-shift of the negative sequence load current changes, being equal to $-2\pi/3$ rad, $2\pi/3$ rad, and 0 rad, for the cases of Fig. 4.16(a)–(c), respectively.

Taking as reference (4.2.27), the minimum CAPF will be obtained when the load negative sequence angle is equal to 0 rad, whereas the maximum is obtained when the angles are either $-2\pi/3$ rad or $2\pi/3$ rad, which is confirmed observing the parallel converter current in Fig. 4.16. Although, it is expected that the CAPF for Fig. 4.16(a) and Fig. 4.16(b) are equal, there are differences due to the line voltage drop that must be compensated by the converters, increasing the equivalent balanced and negative sequence sag, which are different for each scenario. It is important to observe that due to the lower CAPF in Fig. 4.16(c), the series converter is better utilized, requiring lower actuation voltages to compensate for the grid disturbances.

Table 4.2. Grid voltage characteristic for negative sequence interaction.

	Phase a	**Phase b**	**Phase c**
Voltage magnitude	100V	85V	85V
Phase angle	0°	234.2°	125.8°

4.7.3 CAPF reduction methods

Reactive power injection

Results presented in Fig. 4.17 show the response of the HDT when utilizing the reactive power controller. For demonstration purposes, the compensation of the parallel converter is turned off. A resistive load and a power converter injecting 5A of reactive current are utilized. At $t = 50$ms, a 15% voltage sag is applied, and the secondary side voltage is regulated. The results show that the CAPF increases from 26 to 42W due to the additional losses of the power converters. The CAPF in this scenario corresponds to 4.3%, versus the 43% presented in Fig. 4.15(c). Additionally, because of the reactive power compensation, the voltage on the secondary side is shifted with respect to its nominal angle.

DC source connection

The results when a DC source emulating a BESS is connected to the HDT are presented in Fig. 4.18. The parallel converter stops regulating the DC-Link, providing only PF correction. The series converter compensates for the 15% voltage sag applied at $t = 50$ms. The results show that CAPF corresponds to 11W and is unaffected by the voltage sag. In this case, the power provided by the DC source is 123W, corresponding to 15% of the load power plus the power converter losses.

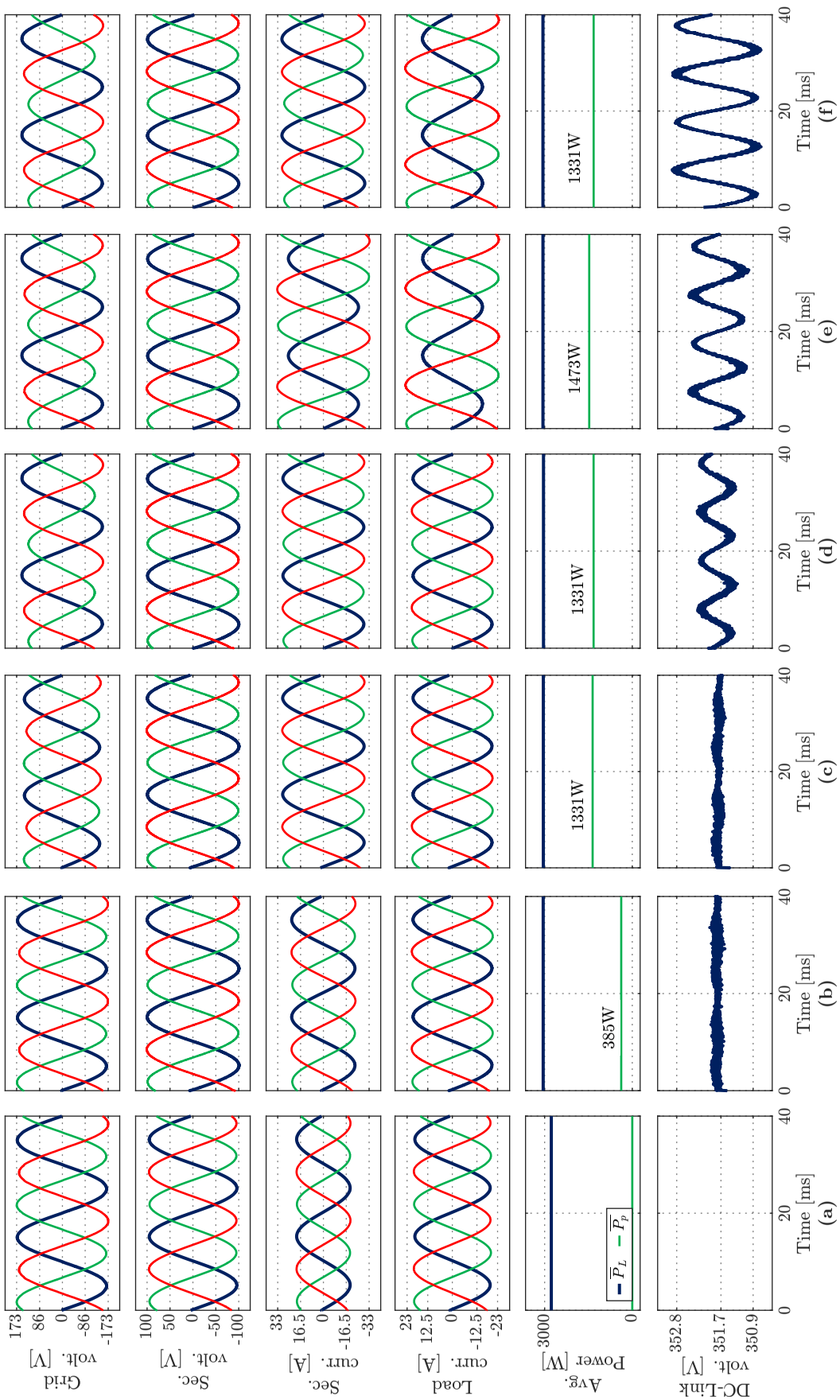


Fig. 4.15. HDT response under different grid conditions. **(a)** Power converters off. **(b)** Normal operation. **(c)** Balanced voltage sag. **(d)** Unbalanced grid voltage.**(e)** Unbalanced load. **(f)** Load compensation.

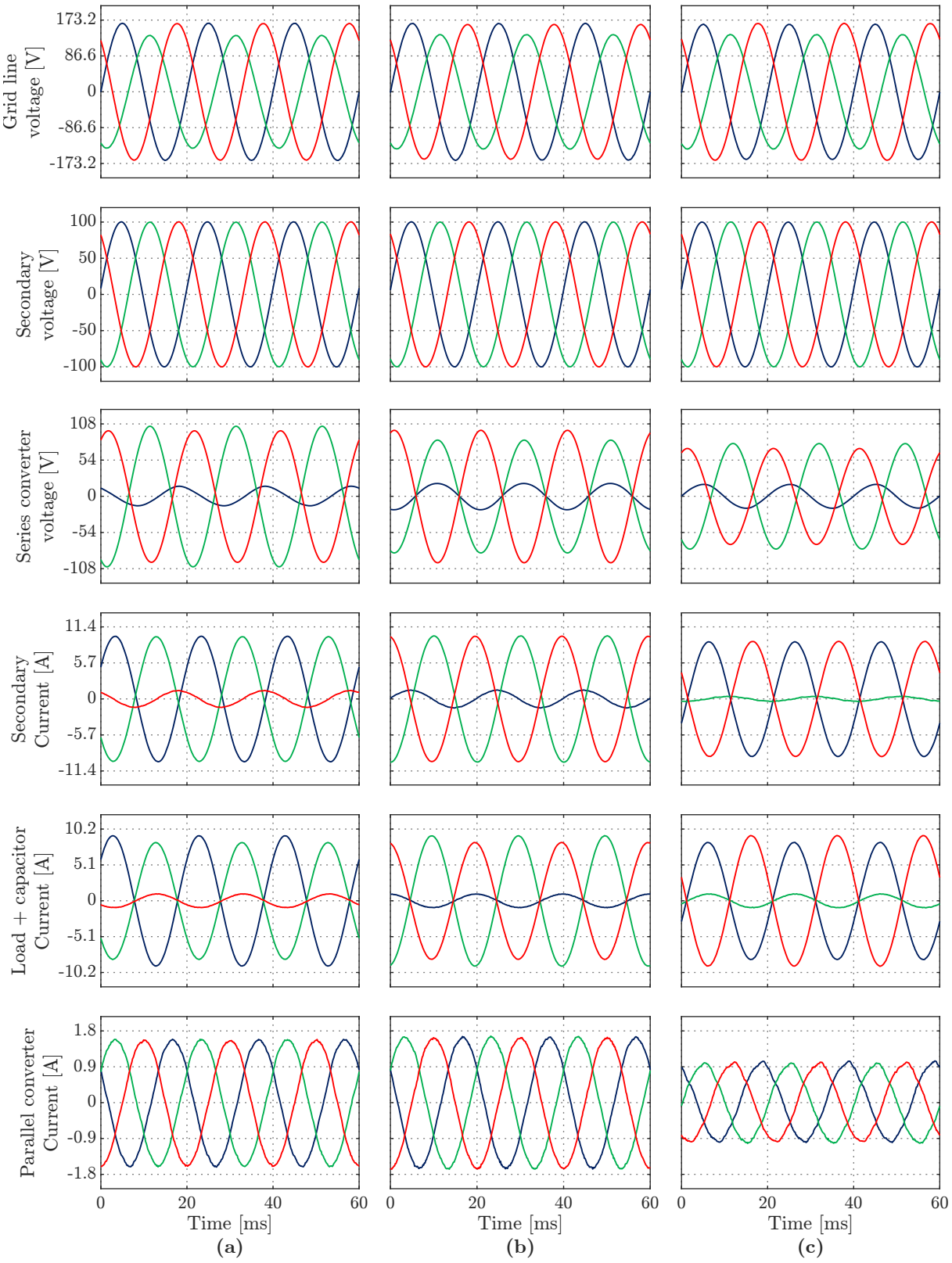


Fig. 4.16. CAPF with a resistive load connected between different phases (Microcontroller) - Example of Fig. 4.5. **(a)** Load connected between phases a and b. **(b)** Load connected between phases b and c. **(c)** Load connected between phases c and a.

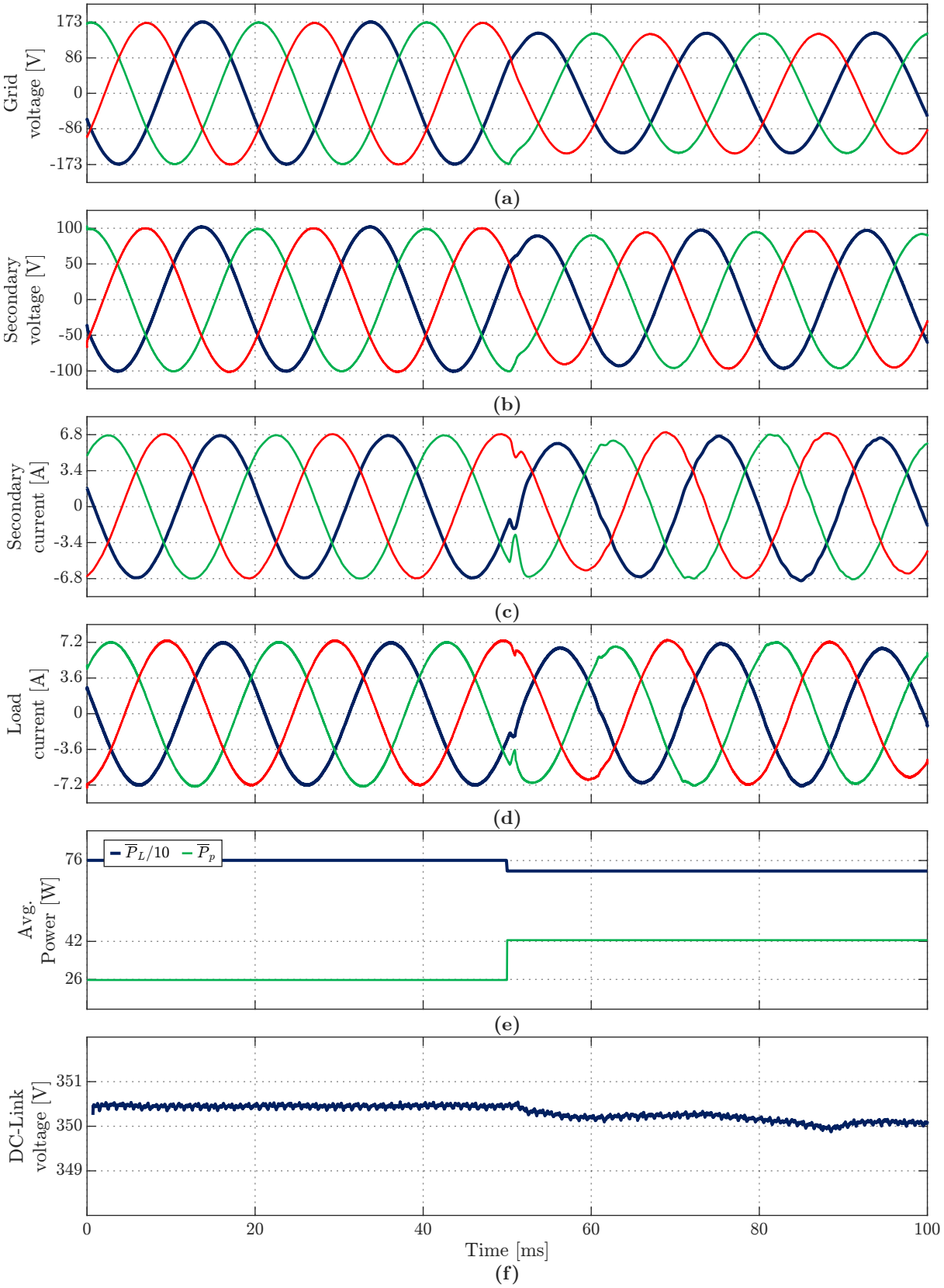


Fig. 4.17. HDT using series reactive power compensation. **(a)** Grid voltage. **(b)** Secondary-side voltage. **(c)** Secondary-side current. **(d)** Load current. **(e)** HDT active power. **(f)** DC-Link voltage.

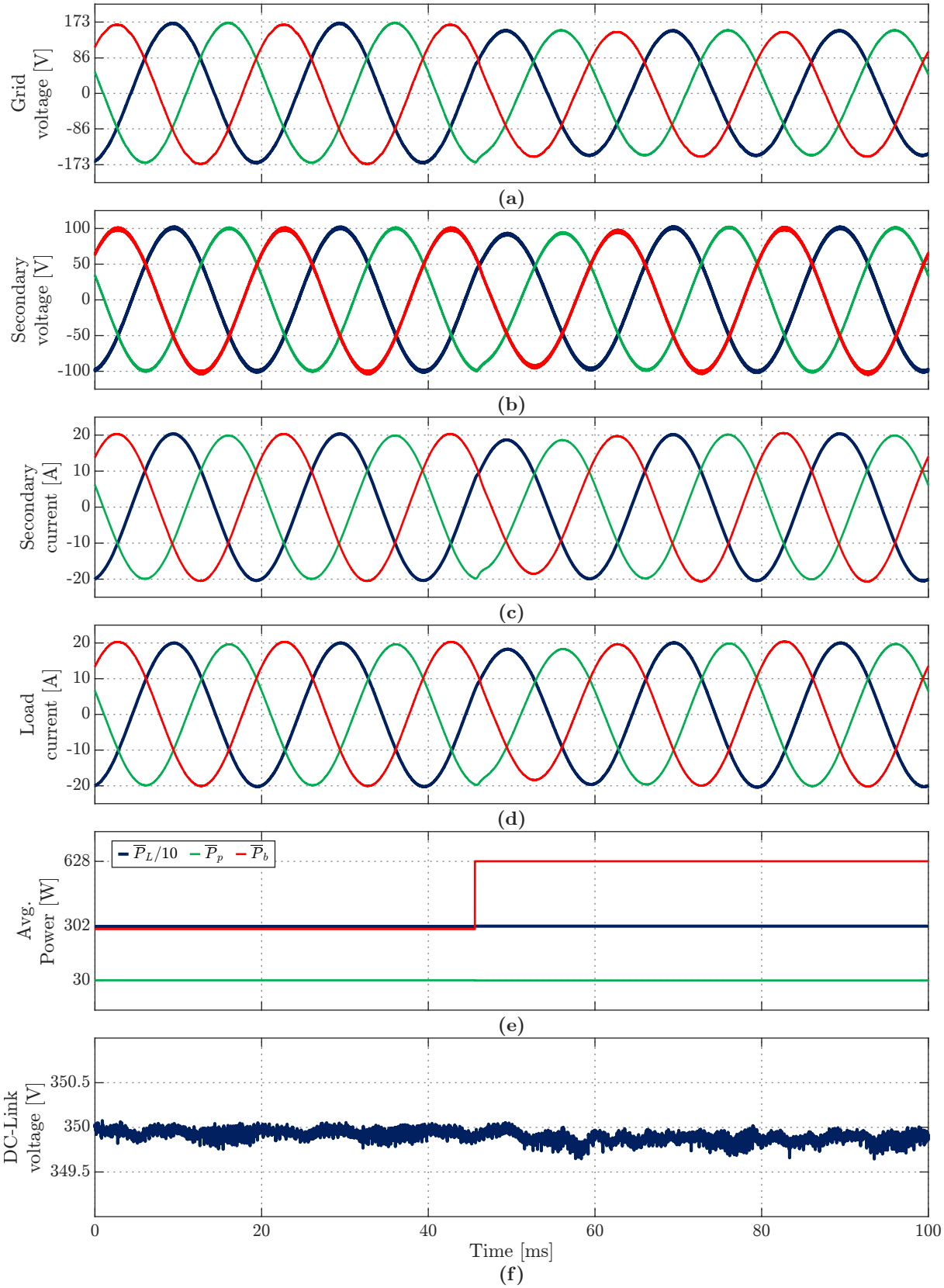


Fig. 4.18. HDT integrating a BESS. **(a)** Grid voltage. **(b)** Secondary-side voltage. **(c)** Secondary-side current. **(d)** Load current. **(e)** HDT active power. **(f)** DC-Link voltage.

4.8 Conclusions

The results presented in this chapter show that in the proposed HDT configurations in which the series converter is connected to the MV side and the parallel converter is connected to the LV side, there is an inevitable CAPF between the LFT and the power converters when the load voltage is controlled to follow the grid voltage angle. The nonlinear relationship between the CAPF and the voltage sag/swell magnitude was confirmed, as well as the interaction of the negative sequence of the compensation voltage and uncompensated unbalanced load current, which can also increase or reduce the CAPF.

Restricting the series converter to inject reactive power to compensate for the grid voltage effectively reduces the CAPF. Nonetheless, the regulation capabilities of the HDT are reduced, and there is a strict relationship between the PF of the load and the amount of sag/swell that the HDT can provide, which is more reduced as the PF increases. Moreover, higher actuation voltages are required to achieve the compensation as the PF increases.

Integrating a BESS into the HDT effectively eliminates the CAPF, as the BESS directly provides all the power required by the series converter. It is a promising solution due to the following benefits:

1. It eliminates the CAPF.
2. It does not affect the phase angle of the secondary side voltage.
3. The injected series voltage magnitude and phase are not attached to the PF.
4. The series power converter is better utilized.

Additionally, incorporating BESS or DC systems can extend the applicability of HDTs to smart grids, which is suitable for modern power systems.

Chapter 5

CONTROL OF THE HDT TO IMPROVE POWER QUALITY

Remark: This chapter is partly based on the following publications of the author:

[1] A. Carreno, M. A. Perez and M. Malinowski, "State-Feedback Control of a Hybrid Distribution Transformer for Power Quality Improvement of a Distribution Grid," in *IEEE Transactions on Industrial Electronics*, 2024.

[2] A. Carreno, M. Perez, C. Baier and J. Espinoza, "Distribution Network Hybrid Transformer for Load Current and Grid Voltage Compensation," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2019.

Based on the model of the HDT presented in **Chapter 2**, a control strategy for the HDT that improves the PQ of the distribution grids is proposed. The control algorithm is based on a discrete-time state feedback controller, which is expanded to include the computation delay and a set of desired harmonics components to be compensated. Additionally, the regulator of the DC-Link voltage, the estimators of the load current, grid voltage, and capacitor voltage of the LC filter are presented.

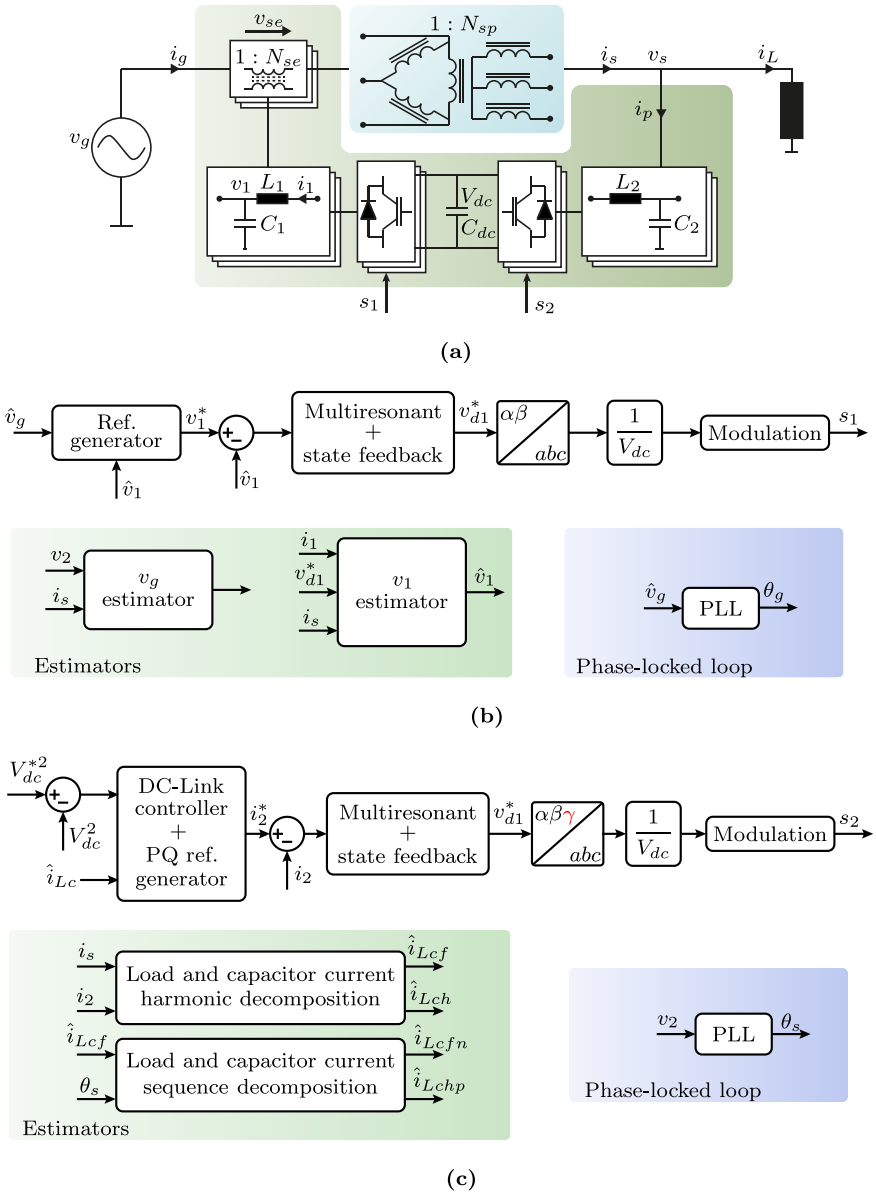


Fig. 5.1. General scheme of the HDT controller. **(a)** HDT diagram. **(b)** Series converter controller. **(c)** Parallel converter controller.

A general representation of the controller of the HDT is shown in Fig. 5.1. The diagrams shown in Fig. 5.1(b) correspond to the controller of the series converter and its corresponding estimators. The capacitor voltage reference is obtained in order to compensate for the estimated grid disturbances. On the other side, the diagram shown in Fig. 5.1(c) corresponds to the parallel converter controller. The power converter output current reference is calculated to regulate the DC-Link voltage and to improve the quality of the secondary-side currents. This control algorithm is done in the $\alpha\beta\gamma$ coordinates. Nonetheless, the γ component is utilized only in the presence of 4-wire distribution grids.

5.1 Series converter controller in $\alpha\beta$ coordinates

This section presents the control algorithm of the series converter. First, the discrete model of the plant is obtained in order to design a state-feedback controller. Then, the capacitor and grid voltage estimators are presented.

There is no neutral connection in the series converter, therefore the control is only done using the $\alpha\beta$ components. Moreover, once the synthesized voltages are injected into the grid, any potential common-mode voltage presented on the CTs or grid is removed due to the $\Delta - Y$ winding configuration of the main LFT.

5.1.1 Discrete model

The discrete model of the series converter is obtained utilizing the ZOH transformation. During the controller design, the disturbance corresponding to the current through the primary winding of the CT is neglected. The discrete model of the continuous system of (2.2.6) in $\alpha\beta$ coordinates is shown as follows.

$$x_{1\alpha\beta}[k+1] = \mathbf{\Phi_1} x_{1\alpha\beta}[k] + \mathbf{\Gamma_1} v_{d1\alpha\beta}[k] \tag{5.1.1}$$

where the matrices $\mathbf{\Phi_1}$ and $\mathbf{\Gamma_1}$ are obtained according to the following equations considering that h is the sampling time.

$$\mathbf{\Phi_1} = e^{\mathbf{A_{c1}}h} \tag{5.1.2a}$$

$$\mathbf{\Gamma_1} = \int_0^h e^{\mathbf{A_{c1}}s} ds \mathbf{B_{c1}} \tag{5.1.2b}$$

The previous matrices can be obtained utilizing a numeric computing environment such as MATLAB. Nonetheless, if the series resistance of the inductor, R_1, and the parallel resistance of the capacitor, R_{c1}, are neglected, the following results for $\mathbf{\Phi_1}$ and $\mathbf{\Gamma_1}$ are obtained.

$$\mathbf{\Phi_1} \approx \begin{bmatrix} \cos(\omega_r h)\mathbf{I} & \omega_r L_1 \sin(\omega_r h)\mathbf{I} \\ \omega_r C_1 \sin(\omega_r h)\mathbf{I} & \cos(\omega_r h)\mathbf{I} \end{bmatrix} \tag{5.1.3a}$$

$$\mathbf{\Gamma_1} \approx \begin{bmatrix} (1 - \cos(\omega_r h))\mathbf{I} \\ \omega_r C_1 \sin(\omega_r h)\mathbf{I} \end{bmatrix} \tag{5.1.3b}$$

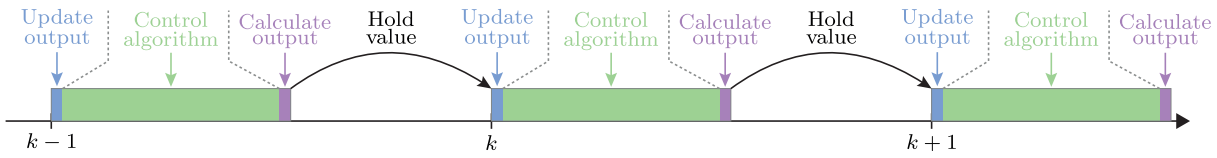


Fig. 5.2. Control algorithm timing diagram.

The previous equations model the LC filter in discrete time.

Adding the computation delay

The diagram presented in Fig. 5.2 shows the time representation of a control algorithm implemented in a digital platform. Basically, at the beginning of each sample period, the output of the system is updated and applied to the PWM modulator. Then, the control algorithm runs and a new output is calculated. This value is held and applied at the beginning of the next sample period. Therefore, there is an intrinsic one-sample delay in digital control systems when the output of the systems is uploaded at the beginning of the period. This phenomenon can be easily modeled in a discrete-time representation.

The one-sample delay can be included in the state-space representation by expanding (5.1.1). The computation delay can be modeled as follows.

$$v_{d1\alpha\beta}[k+1] = v^*_{d1\alpha\beta}[k] \tag{5.1.4}$$

where $v^*_{d1\alpha\beta}[k]$ is the reference output voltage of the power converter, which will be modulated by the PWM during the next sampling period. Then, considering that $v_{d1\alpha\beta}$ is now a state variable, $x_{1e\alpha\beta}$ is the expanded state vector.

$$x_{1e\alpha\beta}[k] = \begin{bmatrix} v_{1\alpha\beta}[k] \\ i_{1\alpha\beta}[k] \\ v_{d1\alpha\beta}[k] \end{bmatrix}, \tag{5.1.5}$$

and the expanded state space model is given as follows.

$$x_{1e\alpha\beta}[k+1] = \mathbf{\Phi_{1e}} x_{1e\alpha\beta}[k] + \mathbf{\Gamma_{1e}} v^*_{d1\alpha\beta}[k] \tag{5.1.6a}$$

$$v_{1\alpha\beta}[k] = \mathbf{C_{1ev1}} x_{1e\alpha\beta}[k] \tag{5.1.6b}$$

$$i_{1\alpha\beta}[k] = \mathbf{C_{1ei1}} x_{1e\alpha\beta}[k] \tag{5.1.6c}$$

where the expanded matrices $\mathbf{\Phi_{1e}}$, $\mathbf{\Gamma_{1e}}$, $\mathbf{C_{1ev1}}$, and $\mathbf{C_{1ev1}}$ are given below.

$$\mathbf{\Phi_{1e}} = \begin{bmatrix} \mathbf{\Phi_1} & \mathbf{\Gamma_1} \\ \mathbf{O} & \mathbf{O} \end{bmatrix} \tag{5.1.7a}$$

$$\mathbf{\Gamma_{1e}} = \begin{bmatrix} \mathbf{O_{4x2}} \\ \mathbf{I} \end{bmatrix} \tag{5.1.7b}$$

$$\mathbf{C_{1ev1}} = \begin{bmatrix} \mathbf{C_{1v1}} & \mathbf{O} \end{bmatrix} \quad \mathbf{C_{1ei1}} = \begin{bmatrix} \mathbf{C_{1i1}} & \mathbf{O} \end{bmatrix} \tag{5.1.7c}$$

The previous equations model the series converter considering the computation delay. The input of the system corresponds to $v^*_{d1\alpha\beta}[k]$, which later will be calculated using state feedback.

5.1.2 Capacitor voltage regulator

The objective of the series converter is the regulation of the load voltage, which is achieved by controlling the fundamental and harmonic components of the capacitor voltage. If a conventional state-feedback controller is designed based on the previous model, there will be an undesirable steady-state error. Therefore, the system must be again expanded, including resonant terms of the capacitor voltage tracking error.

The state-space representation of a system resonating at frequency single frequency ω_i, whose input is the capacitor voltage tracking error, $e_{v1\alpha\beta}[k]$ is given as follows.

$$\rho_{i\alpha\beta}[k+1] = \mathbf{A_{ri}}\rho_i[k] + \mathbf{B_{ri}}e_{v1\alpha\beta}[k], \tag{5.1.8}$$

where $\rho_{i\alpha\beta}[k]$ is the $4x4$ state-vector of the resonant system in $\alpha\beta$ coordinates, and the matrices $\mathbf{A_{ri}}$ and $\mathbf{B_{ri}}$ are shown below.

$$\mathbf{A_{ri}} = \begin{bmatrix} 2\cos(\omega_i h)\mathbf{I} & \text{-}\mathbf{I} \\ \mathbf{I} & \mathbf{O} \end{bmatrix} \tag{5.1.9a}$$

$$\mathbf{B_{ri}} = \begin{bmatrix} \frac{2}{\omega_i^2}(1\text{-}\cos(\omega_i h))\mathbf{I} \\ \mathbf{O} \end{bmatrix} \tag{5.1.9b}$$

Then, based on the previous model, the representation of n resonant systems is given by the state-vector $\rho_{\alpha\beta}[k]$, and the matrices $\mathbf{A_r}$ and $\mathbf{B_r}$.

$$\rho_{\alpha\beta}[k+1] = \mathbf{A_r}\rho_{\alpha\beta}[k] + \mathbf{B_r}e_{v1\alpha\beta}[k] \tag{5.1.10a}$$

$$\mathbf{A_r} = \begin{bmatrix} \mathbf{A_{r1}} & \mathbf{O_{4x4}} & \cdots & \mathbf{O_{4x4}} \\ \mathbf{O_{4x4}} & \mathbf{A_{r2}} & & \mathbf{O_{4x4}} \\ \vdots & & \ddots & \mathbf{O_{4x4}} \\ \mathbf{O_{4x4}} & \mathbf{O_{4x4}} & & \mathbf{A_{rn}} \end{bmatrix} \tag{5.1.10b}$$

$$\mathbf{B_r} = \begin{bmatrix} \mathbf{B_{r1}} \\ \mathbf{B_{r2}} \\ \vdots \\ \mathbf{B_{rn}} \end{bmatrix} \tag{5.1.10c}$$

After coupling the resonant system to the expanded LC state-space representation, the new state vector, $x_{1r\alpha\beta}[k]$, and the output matrix are given as follows.

$$x_{1r\alpha\beta}[k] = \begin{bmatrix} v_{1\alpha\beta}[k] \\ i_{1\alpha\beta}[k] \\ v_{d1\alpha\beta}[k] \\ \rho_{1\alpha\beta}[k] \\ \vdots \\ \rho_{n\alpha\beta}[k] \end{bmatrix} \tag{5.1.11}$$

$$\mathbf{C_{1er}} = \begin{bmatrix} \mathbf{C_{1e}} & \mathbf{O_{2x2n}} \end{bmatrix} \tag{5.1.12}$$

which allow us to write the capacitor voltage error as follows.

$$e_{v1\alpha\beta}[k] = v^*_{1\alpha\beta}[k] - \mathbf{C_{1er}}x_{1er\alpha\beta}[k] \tag{5.1.13}$$

Then, combining the previous equations into one single representation, the following state space model is obtained.

$$x_{1er\alpha\beta}[k+1] = \mathbf{A_{1er}}x_{1er\alpha\beta}[k] + \mathbf{B_{er}}v^*_{d1\alpha\beta}[k] + \mathbf{B_{erv}}v^*_{1\alpha\beta}[k] \tag{5.1.14}$$

where $\mathbf{A_{1er}}$, $\mathbf{B_{er}}$, and $\mathbf{B_{erv}}$ are given as follows.

$$\mathbf{A_{1er}} = \begin{bmatrix} \mathbf{A_{1e}} & \mathbf{O_{6x2n}} \\ \mathbf{B_r C_{1e}} & \mathbf{A_r} \end{bmatrix} \tag{5.1.15a}$$

$$\mathbf{B_{er}} = \begin{bmatrix} \mathbf{B_{1e}} \\ \mathbf{O_{2nx2}} \end{bmatrix} \tag{5.1.15b}$$

$$\mathbf{B_{erv}} = \begin{bmatrix} \mathbf{O_{6x2}} \\ \mathbf{B_r} \end{bmatrix} \tag{5.1.15c}$$

The previous equation models the states of the series converter when the computation delay and a set of resonant terms are added into the system. So far the model consists of two reference inputs. The first one corresponds to the output voltage reference of the power converter $v^*_{d1\alpha\beta}[k]$, whereas the second input corresponds to the capacitor voltage reference $v^*_{1\alpha\beta}[k]$. The resonant terms associated with the capacitor voltage error, do not influence the operation of the power converter, because the controller has not been implemented yet.

The output voltage reference is generated by the state-feedback controller, whose control law is given by the following equation.

$$v^*_{d1\alpha\beta}[k] = -\mathbf{L_g} x_{1er\alpha\beta}[k], \tag{5.1.16}$$

where $\mathbf{L_g}$ corresponds to the state-feedback gain applied to each one of the states of the expanded system. The feedback gain is obtained utilizing an LQR because it simplifies the design process while guaranteeing robust phase and gain margins. For the expanded system, the LQR is such that the feedback gain $\mathbf{L_g}$ minimizes the following cost function.

$$J = \sum_{k=0}^{\infty} (x^T_{1er\alpha\beta} \mathbf{Q_1} x_{1er\alpha\beta} + v^T_{d1\alpha\beta} \mathbf{R_1} v_{d1\alpha\beta}) \tag{5.1.17}$$

The design matrices $\mathbf{Q_1}$ and $\mathbf{R_1}$ are positive definite and they penalize the state variables and control signal. In **Appendix A** the reader can find additional information about the LQR. From now on, the LQR algorithm will be used in the following manner:

$$\mathbf{K} = \mathrm{LQR}(\mathbf{A}, \mathbf{B}, \mathbf{Q}, \mathbf{R}) \tag{5.1.18}$$

which means that the LQR is utilized to design the state-feedback gain $\mathbf{K}$, based on the matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{Q}$, and $\mathbf{R}$.

So far the controller was developed assuming that all the state variables are measured. Nevertheless, the capacitor voltage measurement is not available in the experimental

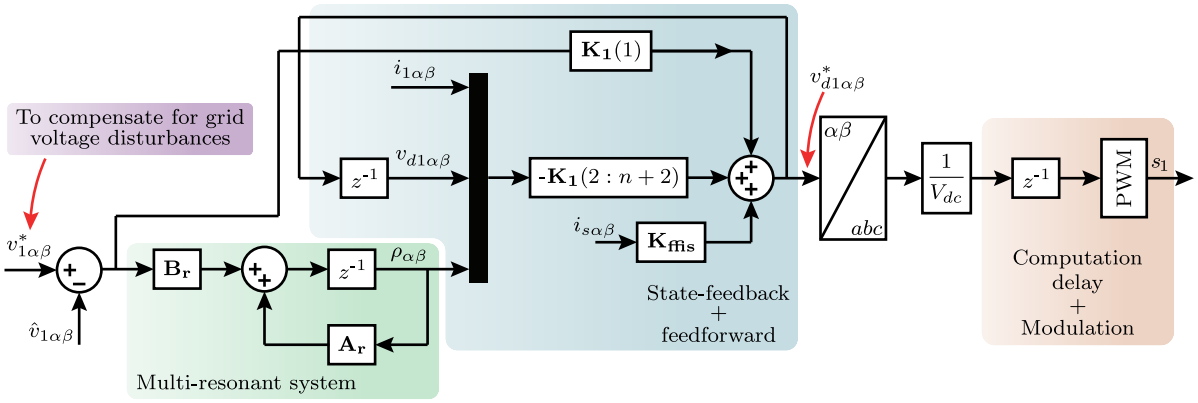


Fig. 5.3. Series converter - Capacitor voltage controller.

implementation. Therefore its estimation, $\hat{v}_{1\alpha\beta}[k]$, and the following state vector are utilized for the state feedback controller.

$$x_{1er\alpha\beta}[k] = \begin{bmatrix} \hat{v}_{1\alpha\beta}[k] \\ i_{1\alpha\beta}[k] \\ \rho_{1\alpha\beta}[k] \\ \vdots \\ \rho_{n\alpha\beta}[k] \end{bmatrix} \tag{5.1.19}$$

The controller is presented in Fig. 5.3. The reference capacitor voltage is calculated in order to compensate for the grid voltage disturbances, as shown in the next sections. After the reference output voltage of the series converter, $v^*_{d1\alpha\beta}][k]$ is generated, the $\alpha\beta$ to *abc* coordinates transformation is applied. The modulation index is obtained by dividing the reference voltage by the DC-Link voltage. Finally, at the next sampling period, the calculated modulation index is to the PWM modulator.

5.1.3 Capacitor voltage observer

The capacitor voltage of the series converter is not measured, and a state observer is employed. This estimator is based on the discrete model of the LC filter and a correction loop based on the power converter output current.

The following observer model is obtained based on the extended discrete model that includes the computation delay presented in (5.1.6). The model considers the grid current as an input disturbance, and a correction term $\nu_{1v1\alpha\beta}[k]$.

$$\hat{x}_{1\alpha\beta}[k+1] = \mathbf{A_{1e}}\hat{x}_{1\alpha\beta}[k] + \mathbf{B_{1e}}v^*_{d1\alpha\beta}[k] + \mathbf{P_{1e}}i_{g\alpha\beta}[k] + \nu_{1v1\alpha\beta}[k] \tag{5.1.20}$$

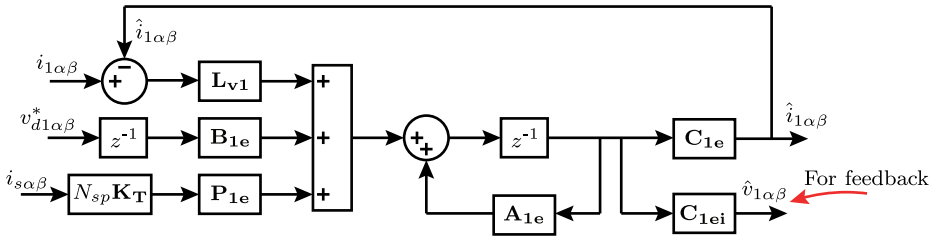


Fig. 5.4. Series converter - Capacitor voltage estimator.

where $\hat{x}_{1\alpha\beta}[k]$ is the estimated state vector which is shown below.

$$\hat{x}_{1\alpha\beta}[k] = \begin{bmatrix} \hat{v}_{1\alpha\beta}[k] \\ \hat{i}_{1\alpha\beta}[k] \\ \hat{v}_{d1\alpha\beta}[k] \end{bmatrix} \tag{5.1.21}$$

The grid current is not measured, but it can estimated and written in terms of the secondary side current using (2.4.9), considering the turns ratio and a rotation matrix. The correction term utilizes the converter current error as follows.

$$\nu_{1v1\alpha\beta}[k] = \mathbf{L_{v1}}(i_{1\alpha\beta}[k] - \hat{i}_{1\alpha\beta}[k]) \tag{5.1.22}$$

where $\hat{i}_{1\alpha\beta}[k] = \mathbf{C_{1ei1}}\hat{x}_{1\alpha\beta}[k]$, and the feedback matrix $\mathbf{L_{v1}}$ is calculated utilizing the LQR algorithm, as follows.

$$\mathbf{L}^{\mathbf{T}}_{\mathbf{v1}} = \mathrm{LQR}(\mathbf{A}^{\mathbf{T}}_{\mathbf{1e}}, \mathbf{C}^{\mathbf{T}}_{\mathbf{1ei1}}, \mathbf{Q_{\hat{v}1}}, \mathbf{R_{\hat{v}1}}), \tag{5.1.23}$$

where $\mathbf{Q_{\hat{v}1}}$ and $\mathbf{R_{\hat{v}1}}$ are the design matrices.

Once the state is estimated, the observed capacitor voltage is used as a feedback term in the capacitor voltage control, utilizing $\hat{v}_{1\alpha\beta}[k] = \mathbf{C_{1ev1}}\hat{x}_{1\alpha\beta}[k]$. The diagram of the capacitor voltage estimator is shown in Fig. 5.4. The closed-loop equation of the observer is given by the following equation.

$$\hat{x}_{1\alpha\beta}[k+1] = (\mathbf{A_{1e}} - \mathbf{L_{v1}}\mathbf{C_{1ei1}})\hat{x}_{1\alpha\beta}[k] + \mathbf{B_{1e}}v^*_{d1\alpha\beta}[k] + \mathbf{P_{1e}}i_{g\alpha\beta}[k] + \mathbf{L_{v1}}i_{1\alpha\beta} \tag{5.1.24}$$

where the poles of the system are altered by $\mathbf{L_{v1}}$ in order to decrease the estimation error to zero. The poles are given by the expression $\det(s\mathbf{I} - (\mathbf{A_{1e}} - \mathbf{L_{v1}}\mathbf{C_{1ei1}})) = 0$.

5.1.4 Grid voltage estimator

The capacitor voltage reference is utilized to mitigate the disturbances of the grid voltage, in order to improve the voltage quality on the load side and in the terminals of the main LFT. The grid voltage is not measured in this chapter. Therefore, its estimation is necessary.

The estimator is based on the equivalent circuit of the secondary side of the LFT, which is modeled by the following equation.

$$\frac{\mathrm{d}i_s}{\mathrm{d}t} = -\frac{R_s}{L_s}i_s - \frac{1}{L_s}v_2 + \frac{1}{L_s}v_x \tag{5.1.25}$$

The discrete model is obtained using the ZOH transformation considering that the state corresponds to i_s, and the input to v_2. The discrete-time state matrices are $\mathbf{A_g}$ and $\mathbf{B_g}$.

While i_s and v_2 are directly measured, the induced voltage of the transformer, v_x, is not available. Therefore, the first task of the observer is to estimate v_x. This task is done utilizing a multiresonant system, which states are modeled as follows.

$$\rho_{vx\alpha\beta}[k+1] = \mathbf{A_r}\rho_{vx\alpha\beta}[k] + \nu_{vx\alpha\beta}[k] \tag{5.1.26}$$

where $\rho_{vx\alpha\beta}[k]$ are the internal states of the resonant systems that model the induced voltage, $\nu_{vx\alpha\beta}[k]$ is a correction term that depends on $i_{s\alpha\beta}[k]$. The output of the resonant system corresponds to the estimated value of the induced voltage, $\hat{v}_{x\alpha\beta}[k]$, as shown below.

$$\hat{v}_x[k] = \mathbf{C_r}\rho[k] \tag{5.1.27a}$$

$$\mathbf{C_r} = \begin{bmatrix}\mathbf{C_{r1}} & \mathbf{C_{r2}} & \cdots & \mathbf{C_{rn}}\end{bmatrix} \tag{5.1.27b}$$

$$\mathbf{C_{ri}} = \begin{bmatrix}\mathbf{I} & \mathbf{O}\end{bmatrix} \tag{5.1.27c}$$

Combining the model of the secondary current and the resonant system into one single state space representation, while considering the estimated induced voltage, the following expression is obtained.

$$\hat{x}_{g\alpha\beta}[k+1] = \mathbf{A_{gr}}\hat{x}_{g\alpha\beta}[k] + \mathbf{B_{gr}}v_{s\alpha\beta}[k] - \mathbf{B_{gr}}\hat{v}_{x\alpha\beta}[k] + \nu_{vx\alpha\beta}[k], \tag{5.1.28}$$

where the state vector and matrices are the following.

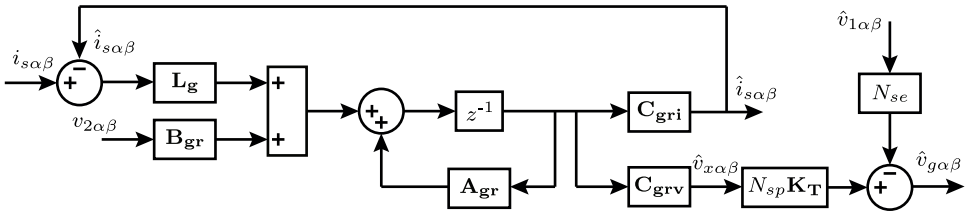


Fig. 5.5. Series converter - Grid voltage estimator.

$$\hat{x}_{g\alpha\beta} = \begin{bmatrix} \hat{i}_{s\alpha\beta} \\ \rho_{vx1\alpha\beta} \\ \vdots \\ \rho_{vxn\alpha\beta} \end{bmatrix} \tag{5.1.29a}$$

$$\mathbf{A_{gr}} = \begin{bmatrix} \mathbf{A_g} & \mathbf{B_g C_r} \\ \mathbf{O_{2x2n}} & \mathbf{A_r} \end{bmatrix} \tag{5.1.29b}$$

$$\mathbf{B_{gr}} = \begin{bmatrix} \mathbf{B_g} \\ \mathbf{O_{2nx2}} \end{bmatrix} \tag{5.1.29c}$$

Based on the previous matrix definitions, the estimated current and voltage are $\hat{i}_{s\alpha\beta}[k] = \mathbf{C_{gri}}\hat{x}_{g\alpha\beta}[k]$ and $\hat{v}_{x\alpha\beta}[k] = \mathbf{C_{grv}}\hat{x}_{g\alpha\beta}[k]$, where $\mathbf{C_{gri}} = \begin{bmatrix} \mathbf{I} & \mathbf{O_{2x2n}} \end{bmatrix}$ and $\mathbf{C_{grv}} = \begin{bmatrix} \mathbf{O} & \mathbf{C_r} \end{bmatrix}$. The secondary side current is measured and used as a correction term in the observer, as follows.

$$\nu_{vx\alpha\beta}[k] = \mathbf{L_g}(i_{s\alpha\beta}[k] - \hat{i}_{s\alpha\beta}[k]) \tag{5.1.30}$$

where $\mathbf{L_g}$ is designed using $\mathbf{L_g^T} = \text{LQR}(\mathbf{A_{gr}^T}, \mathbf{C_{gri}^T}, \mathbf{Q_{\hat{v}x}}, \mathbf{R_{\hat{v}x}})$, with the matrices $\mathbf{Q_{\hat{v}x}}$ and $\mathbf{R_{\hat{v}x}}$ as design parameters.

Once $\hat{v}_{x\alpha\beta}[k]$ is obtained, it is transferred to the MV side of the LFT by multiplying by the turns ratio and the transformation matrix. To the result of this operation, the estimation of the capacitor voltage multiplied by the winding ratio of the CT is subtracted to obtain the estimated grid voltage. The estimated grid voltage is shown as follows.

$$\hat{v}_{g\alpha\beta}[k] = \frac{1}{N_{sp}}\mathbf{K_T}\hat{v}_{x\alpha\beta}[k] - N_{se}\hat{v}_{1\alpha\beta}[k] \tag{5.1.31}$$

A PLL is applied to the estimated grid voltage to obtain the phase angle of the positive sequence component, θ_g. Then, the capacitor voltage reference compensates for the grid

voltage disturbances, i.e., harmonics and fundamental disturbances. The reference is obtained as follows.

$$v^*_{1\alpha\beta}[k] = |V_n| \begin{bmatrix} \cos(\theta_g) \\ \sin(\theta_g) \end{bmatrix} - \hat{v}_{g\alpha\beta}[k] \tag{5.1.32}$$

where $|V_n|$ is the rated voltage of the grid. The estimator diagram is summarized in Fig. 5.5.

5.2 Parallel converter controller in $\alpha\beta\gamma$ coordinates

A similar approach as the one followed for the series controller is applied to the parallel controller, i.e., a multi-resonant state-feedback controller taking into consideration the computation delay. The controller regulates the converter current, whose reference is set up to mitigate the load and capacitor harmonics and negative sequence components, in conjunction with controlling the DC-Link voltage. An observer is applied to decompose the load current into its fundamental and harmonic components, where the former is processed to obtain its positive and negative sequence.

The current controller of the parallel converter is presented in Fig. 5.6. In the case of neutral wire connection, the controller considers the γ component of the converter current.

5.2.1 Discrete model

Model in $\alpha\beta$ coordinates

Following the same steps as in the case of the series converter, the discrete-time model of the LCL filter of (2.3.5) is given as follows.

$$x_{2\alpha\beta}[k+1] = \mathbf{\Phi_2} x_{1\alpha\beta}[k] + \mathbf{\Gamma_2} v_{d2\alpha\beta}[k] \tag{5.2.1}$$

where the matrices $\mathbf{\Phi_2}$ and $\mathbf{\Gamma_2}$ are obtained utilizing the ZOH transformation.

$$\mathbf{\Phi_2} = e^{\mathbf{A_{c2}}h} \tag{5.2.2a}$$

$$\mathbf{\Gamma_2} = \int_0^h e^{\mathbf{A_{c2}}s} ds \mathbf{B_{c2}} \tag{5.2.2b}$$

The previous equation can be simplified if the damping elements, such as the series and

parallel resistance of the inductors and capacitors, respectively, are neglected.

$$\mathbf{\Phi_2} \approx \begin{bmatrix} \frac{L_s\cos(\omega_r h)+L_2}{L_2+L_s}\mathbf{I} & \frac{L_s(\cos(\omega_r h)-1)}{L_2+L_s}\mathbf{I} & \frac{\sin(\omega_r h)}{L_2\omega_r}\mathbf{I} \\ \frac{L_s(\cos(\omega_r h)-1)}{L_2+L_s}\mathbf{I} & \frac{L_2\cos(\omega_r h)+L_s}{L_2+L_s}\mathbf{I} & \frac{\sin(\omega_r h)}{L_s\omega_r}\mathbf{I} \\ \frac{\sin(\omega_r h)}{\omega_r C_2}\mathbf{I} & \frac{\sin(\omega_r h)}{\omega_r C_2}\mathbf{I} & \cos(\omega_r h)\mathbf{I} \end{bmatrix} \tag{5.2.3a}$$

$$\mathbf{\Gamma_2} \approx \begin{bmatrix} \left(\frac{L_s\sin(\omega_r h)}{L_2(L_2+L_s)\omega_r}+\frac{h}{L_2+L_s}\right)\mathbf{I} \\ \left(\frac{\sin(\omega_r h)}{(L_2+L_s)\omega_r}-\frac{h}{L_2+L_s}\right)\mathbf{I} \\ -\frac{L_s(\cos(\omega_r h)-1)}{L_2+L_s}\mathbf{I} \end{bmatrix} \tag{5.2.3b}$$

The one-sample delay can be included in the state-space representation of (5.2.1) by expanding the initial state-space representation considering that v_{d2} is now a state variable. The expanded state vector is shown as follows.

$$x_{2e\alpha\beta}[k] = \begin{bmatrix} i_{2\alpha\beta}[k] \\ i_{s\alpha\beta}[k] \\ v_{2\alpha\beta}[k] \\ v_{d2\alpha\beta}[k] \end{bmatrix}, \tag{5.2.4}$$

and the expanded state space model is given as follows.

$$x_{2e\alpha\beta}[k+1] = \mathbf{\Phi_{2e}} x_{2e\alpha\beta}[k] + \mathbf{\Gamma_{2e}} v^*_{d2\alpha\beta}[k] \tag{5.2.5a}$$

$$i_{2\alpha\beta}[k] = \mathbf{C_{2ei2}} x_{2e\alpha\beta}[k] \tag{5.2.5b}$$

$$\tag{5.2.5c}$$

where the expanded matrices $\mathbf{\Phi_{2e}}$, $\mathbf{\Gamma_{2e}}$, and $\mathbf{C_{2ei2}}$ are given below.

$$\mathbf{\Phi_{2e}} = \begin{bmatrix} \mathbf{\Phi_2} & \mathbf{\Gamma_2} \\ \mathbf{O} & \mathbf{O} \end{bmatrix} \tag{5.2.6a}$$

$$\mathbf{\Gamma_{2e}} = \begin{bmatrix} \mathbf{O_{6x2}} \\ \mathbf{I} \end{bmatrix} \tag{5.2.6b}$$

$$\mathbf{C_{2ei2}} = \begin{bmatrix} \mathbf{C_{2i2}} & \mathbf{O} \end{bmatrix} \tag{5.2.6c}$$

The previous equations model the series converter considering the computation delay. The input of the system corresponds to $v^*_{d2\alpha\beta}[k]$, which is later calculated using state feedback.

Model in γ coordinates

Based on the model of (2.3.10) and following the same steps as for the $\alpha\beta$ components, the following discrete-time model for the γ component is obtained.

$$x_{2e\gamma}[k+1] = \mathbf{\Phi_{2e\gamma}} x_{2e}[k] + \mathbf{\Gamma_{2e\gamma}}(v^*_{d2\gamma}[k] - v^*_{d2n}[k]) \tag{5.2.7a}$$

$$i_{2\gamma}[k] = \mathbf{C_{2ei2\gamma}} x_{2e\gamma}[k] \tag{5.2.7b}$$

$$\tag{5.2.7c}$$

,

where the state vector is given as follows.

$$x_{2e\gamma}[k] = \begin{bmatrix} i_{2\gamma}[k] \\ i_{s\gamma}[k] \\ v_{2\gamma}[k] \\ v_{d2\gamma}[k] - v_{d2n}[k] \end{bmatrix} \tag{5.2.8}$$

The model considers the one-sample delay of the difference between the γ component and the neutral leg voltage ($v_{d2\gamma}[k] - v_{d2n}[k]$). The system matrices are given as follows.

$$\mathbf{\Phi_{2e\gamma}} = \begin{bmatrix} \mathbf{\Phi_{2\gamma}} & \mathbf{\Gamma_{2\gamma}} \\ 0 & 0 \end{bmatrix} \tag{5.2.9a}$$

$$\mathbf{\Gamma_{2e\gamma}} = \begin{bmatrix} \mathbf{O_{3x1}} \\ 1 \end{bmatrix} \tag{5.2.9b}$$

$$\mathbf{C_{2ei2\gamma}} = \begin{bmatrix} \mathbf{C_{2i2\gamma}} & 0 \end{bmatrix} \tag{5.2.9c}$$

5.2.2 Current controller

The task of the current controller is to regulate the power converter output current in order to:

1. Regulate the DC-Link voltage.

2. Provide harmonic regulation, power factor correction and negative sequence mitigation on the secondary side currents.

3. Remove the zero sequence, or common mode components of the secondary-side currents.

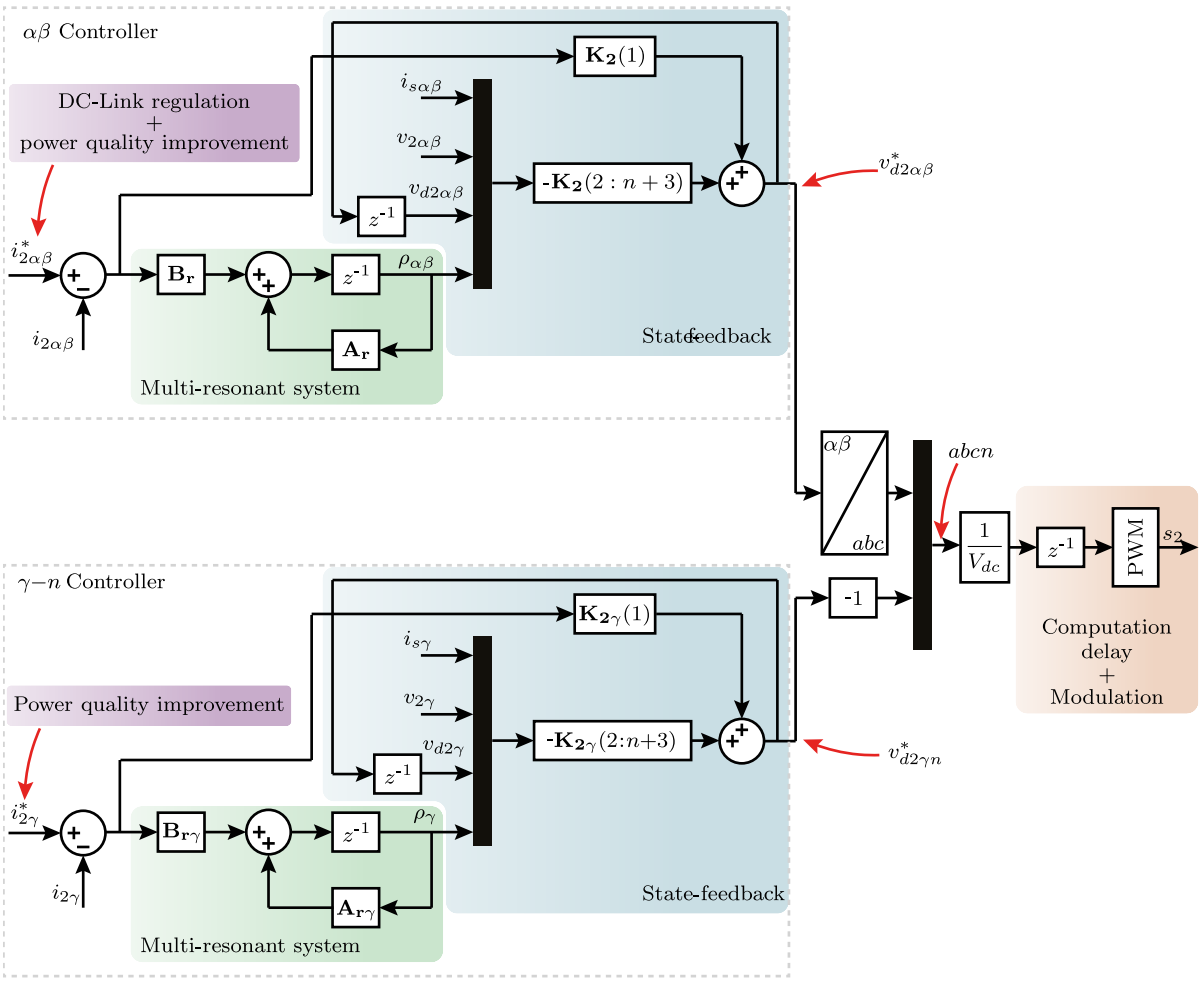
Task 1 and 2 are carried out in the $\alpha\beta$ reference frame, while task 3 is in the γ reference frame. The internal current controllers and the DC-Link regulator are shown in Fig. 5.6.

Based on the discrete $\alpha\beta$ model of (5.2.5), the system input corresponds to $v^*_{d2\alpha\beta}[k]$, whereas the system input for the γ components $v^*_{d2\gamma n}[k] = v^*_{d2\gamma}[k] - v^*_{d2n}[k]$, according to (5.2.7). The last stage of the controller, in which the *abcn* reference signals are obtained, can be done in two different, but equivalent, ways:

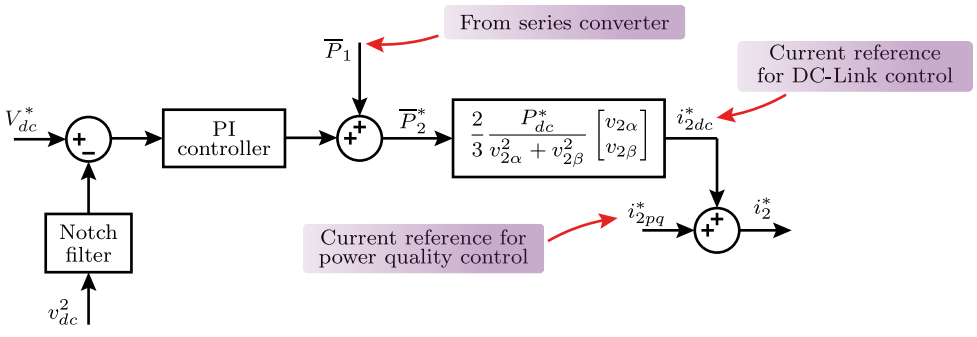
1. Take $v^*_{d2\alpha\beta}$, and apply the $\alpha\beta$ to *abc* transformation. Then, apply a common-mode signal, such as min-max, which is equivalent to adding a γ component, $v^*_{d2\gamma}$. Then, take the output of the γ component controller, and obtain the neutral leg reference voltage as $v^*_{d2n} = -v^*_{d2\gamma n} + v^*_{d2\gamma}$. By doing this, the voltage reference for the a, b, c, and n legs are obtained. Then, the references are sent to the modulator after scaling them by the DC-Link voltage.

2. Take $v^*_{d2\alpha\beta}$, and apply the $\alpha\beta$ to *abc* transformation. Then, take the output of the γ component controller, and obtain the neutral leg reference voltage as $v^*_{d2n} = -v^*_{d2\gamma n}$ by forcing $v^*_{d2\gamma} = 0$. The temporary output voltage references are obtained for the a, b, c, and n legs. After this, the signals are scaled down by the DC-Link voltage and applied to the modulator. If min-max modulation is utilized, it is equivalent to adding a common-mode voltage or γ component. Therefore, the neutral leg modulation index must be updated to compensate the for γ component as $m^*_{d2n} = -m^*_{d2\gamma n} + m^*_{d2\gamma}$.

In this work, the approach number 2 is used as shown in Fig. 5.6(a).



(a)



(b)

Fig. 5.6. Parallel converter - converter current controller. **(a)** Internal $\alpha\beta$ and γ coordinates current controller. **(b)** DC-Link voltage regulator.

$\alpha\beta$ components controller

This section summarizes the state-feedback controller, which follows the same steps as those applied to the series controller.

The following equation shows the open-loop state-space representation of the parallel converter. The system considers the one-sample delay model and a multiresonant system is applied to the converter current error.

$$x_{2er\alpha\beta}[k+1] = \mathbf{A_{2er}} x_{2er\alpha\beta}[k] + \mathbf{B_{2er}} v^*_{d2\alpha\beta}[k] + \mathbf{B_{2eri}} i^*_{2\alpha\beta}[k] \tag{5.2.10}$$

where $\mathbf{A_{2er}}$, $\mathbf{B_{2er}}$, and $\mathbf{B_{2eri}}$ are given as follows.

$$\mathbf{A_{2er}} = \begin{bmatrix} \mathbf{A_{2e}} & \mathbf{O_{8x2n}} \\ \mathbf{B_r C_{2e}} & \mathbf{A_r} \end{bmatrix} \tag{5.2.11a}$$

$$\mathbf{B_{2er}} = \begin{bmatrix} \mathbf{B_{2e}} \\ \mathbf{O_{2nx2}} \end{bmatrix} \tag{5.2.11b}$$

$$\mathbf{B_{2eri}} = \begin{bmatrix} \mathbf{O_{8x2}} \\ \mathbf{B_r} \end{bmatrix} \tag{5.2.11c}$$

and the state vector is given as follows.

$$x_{2er\alpha\beta}[k] = \begin{bmatrix} i_{2\alpha\beta}[k] \\ i_{s\alpha\beta}[k] \\ v_{2\alpha\beta}[k] \\ v_{d2\alpha\beta}[k] \\ \rho_{1\alpha\beta}[k] \\ \vdots \\ \rho_{n\alpha\beta}[k] \end{bmatrix} \tag{5.2.12}$$

The parallel converter current controller in $\alpha\beta$ coordinates is shown in Fig. 5.6(a). The power converter current reference, $i^*_{2\alpha\beta}[k]$, comes from the DC-Link controller and from the AC PQ compensator. The PQ reference is made of the harmonics, reactive currents, and negative sequence current references, respectively. The current reference to improve the PQ comes from the harmonics and sequence estimator, which are presented in the following sections.

Due to the state feedback control law, the output voltage reference is given by

$$v^*_{d2\alpha\beta}[k] = -\mathbf{K_2} x_{2er\alpha\beta}[k] \tag{5.2.13}$$

where $\mathbf{K_2}$ is obtained by applying the LQR algorithm, such that $\mathbf{K_2} = \text{LQR}(\mathbf{A_{2er}}, \mathbf{B_{2er}}, \mathbf{Q}, \mathbf{R})$. The matrices $\mathbf{Q}$ and $\mathbf{R}$ correspond to the design matrices that weights the state error and the input action.

γ component controller

The open-loop γ component model of the LCL considering the sample delay and resonant terms is given below.

$$x_{2er\gamma}[k+1] = \mathbf{A_{2er\gamma}} x_{2er\gamma}[k] + \mathbf{B_{2er}}(v^*_{d2\gamma}[k] - v^*_{d2n}[k]) + \mathbf{B_{2eri\gamma}} i^*_{2\gamma}[k] \tag{5.2.14}$$

where $\mathbf{A_{2er\gamma}}$, $\mathbf{B_{2er\gamma}}$, and $\mathbf{B_{2eri\gamma}}$ are given as follows.

$$\mathbf{A_{2er\gamma}} = \begin{bmatrix} \mathbf{\Phi_{2e\gamma}} & \mathbf{O_{8x2n}} \\ \mathbf{B_r C_{2e\gamma}} & \mathbf{A_r} \end{bmatrix} \tag{5.2.15a}$$

$$\mathbf{B_{2er\gamma}} = \begin{bmatrix} \mathbf{\Gamma_{2e\gamma}} \\ \mathbf{O_{2nx2}} \end{bmatrix} \tag{5.2.15b}$$

$$\mathbf{B_{2eri\gamma}} = \begin{bmatrix} \mathbf{O_{8x2}} \\ \mathbf{B_r} \end{bmatrix} \tag{5.2.15c}$$

and the state vector is given as follows.

$$x_{2er\gamma}[k] = \begin{bmatrix} i_{2\gamma}[k] \\ i_{s\gamma}[k] \\ v_{2\gamma}[k] \\ v_{d2\gamma}[k] - v_{d2n}[k] \\ \rho_{1\gamma}[k] \\ \vdots \\ \rho_{n\gamma}[k] \end{bmatrix} \tag{5.2.16}$$

The parallel converter current controller for the γ component is shown in Fig. 5.6(a). The power converter current reference, $i^*_{2\gamma}[k]$, AC PQ compensator. The PQ reference corresponds to the common mode currents that are present on the load current.

The converter output voltage reference is given by

$$v^*_{d2\gamma}[k] - v^*_{d2n}[k] = -\mathbf{K_{2\gamma}} x_{2er\gamma}[k] \tag{5.2.17}$$

where $\mathbf{K_{2\gamma}}$ is generated by applying the LQR algorithm, such that $\mathbf{K_{2\gamma}} = \text{LQR}(\mathbf{A_{2er\gamma}}, \mathbf{B_{2er\gamma}}, \mathbf{Q}, \mathbf{R})$. The matrices $\mathbf{Q}$ and $\mathbf{R}$ correspond to the design matrices.

5.2.3 DC-Link controller

The main task of the parallel converter is the regulation of the DC-Link voltage, which is fundamental for the correct operation of the HDT. The control algorithm is presented in Fig. 5.6(b). The controller supplies the required active power demanded by the series converter and it also compensates for the system losses to keep the power balance across the DC-Link. The control is based on the energy model of the DC-Link, which has the advantage of providing a linear relationship between the capacitor energy and the power reference. The continuous-time model is presented in (2.3.17), and it is utilized to design the following discrete PI controller.

$$x_{vdcPI}[k{+}1] = x_{vdcPI}[k] + (V^{*2}_{dc}[k] - v^2_{filt}[k]) \tag{5.2.18a}$$

$$\overline{P}^*_2[k] = K_{vdci} x_{vdcPI}[k] + K_{vdcp}(V^{*2}_{dc}[k] - v^2_{filt}[k]) + \overline{P}^*_1[k] \tag{5.2.18b}$$

The output of the controller corresponds to the active power reference required to regulate the DC-Link. The current reference can be obtained utilizing the Instant Power Theory (IPT).

$$i^*_{2dc}[k] = \frac{2}{3} \frac{P^*_{dc}[k]}{v^2_{2\alpha}[k] + v^2_{2\beta}[k]} \begin{bmatrix} v_{2\alpha}[k] \\ v_{2\beta}[k] \end{bmatrix} \tag{5.2.19}$$

There are low-frequency oscillations when operating under a distorted grid or supplying nonlinear loads. Therefore, filters are required only to control the mean value of v^2_{dc}. The use of notch filters has been applied [89], in conjunction with a low-pass filter [98]. The filters can be taken into consideration for the design of the PI controller. In this work, a notch filter is applied to v^2_{dc}, which is tuned to the second harmonic. This filter is written as the following generalized discrete state space representation.

$$x_{1notch}[k{+}1] = K_{notch11} x_{1notch}[k] + K_{notch12} x_{2notch}[k] + K_{notch13} v^2_{dc}[k] \tag{5.2.20a}$$

$$x_{2notch}[k+1] = K_{notch21}x_{1notch}[k] + K_{notch22}x_{2notch}[k] + K_{notch32}v_{dc}^2[k] \tag{5.2.20b}$$

$$v_{filt}^2[k] = K_{notch31}x_{1notch}[k] + K_{notch32}x_{2notch}[k] + K_{notch33}v_{dc}^2[k] \tag{5.2.20c}$$

To improve the transient response of the DC-Link controller, the average output power of the series converter, P_1 or P_{se}, is used as a feedforward term.

5.2.4 Load current harmonic decomposition

As stated before, the converter current is used to mitigate the load and capacitor harmonics, negative sequence, and orthogonal currents. Because the power converter current is controlled, the load and filter capacitor current are supplied by the grid. The latter generates reactive power or even harmonics, degrading the PQ. The current flowing through the load and capacitor is given as $i_{Lc} = i_L + i_c$, which can be estimated as follows.

$$i_{Lc} = i_2 + i_s \tag{5.2.21}$$

Therefore, the power converter current is utilized to mitigate the impacts of the capacitor currents and the undesirable components of the load on the grid.

The harmonic decomposition algorithm is applied to i_{Lc} in the $\alpha\beta$ coordinates, based on the harmonic generator. The estimated current $\hat{i}_{Lc\alpha\beta}$ is obtained from a multi-resonant system whose state matrix has the same structure as the one used for the resonant controller. The $i_{Lc\alpha\beta}$ generator is given by $\rho_{\alpha\beta}[k+1] = \mathbf{A_{iLc}}\rho_{\alpha\beta}[k] + h_{\alpha\beta}[k]$, where $\rho_{\alpha\beta}[k]$ are the states of the harmonic generator and $h[k]$ is a correction term. The estimated fundamental and harmonics currents, $\hat{i}_{Lcf\alpha\beta}[k]$ and $\hat{i}_{Lch\alpha\beta}[k]$, can be written using the following expressions.

$$\hat{i}_{Lcf\alpha\beta}[k] = \underbrace{\begin{bmatrix}\mathbf{C_{r1}} & \mathbf{O_{2(n-1)x2}}\end{bmatrix}}_{\mathbf{C_f}} \rho_{\alpha\beta}[k] \tag{5.2.22a}$$

$$\hat{i}_{Lch\alpha\beta}[k] = \underbrace{\begin{bmatrix}\mathbf{O_{4x2}} & \mathbf{C_{r2}} & \cdots & \mathbf{C_{rn}}\end{bmatrix}}_{\mathbf{C_h}} \rho_{\alpha\beta}[k] \tag{5.2.22b}$$

Then, the total estimated current is given as follows.

$$\hat{i}_{Lc\alpha\beta}[k] = \mathbf{C_{iLc}}\rho_{\alpha\beta}[k] \tag{5.2.23a}$$

$$\mathbf{C_{iLc}} = \mathbf{C_f} + \mathbf{C_h} \tag{5.2.23b}$$

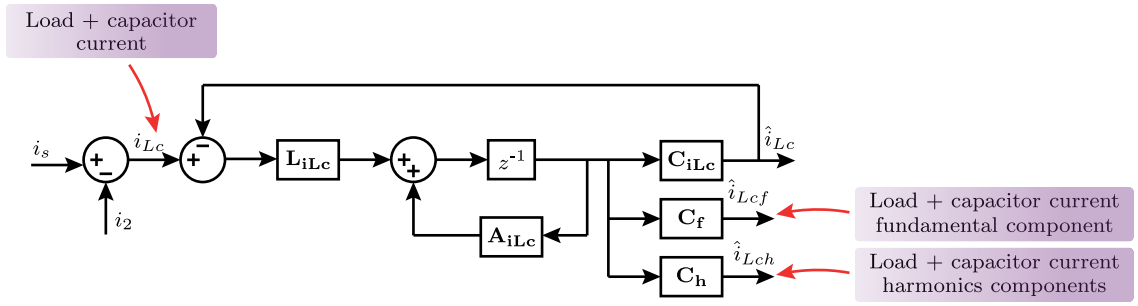


Fig. 5.7. Parallel converter - Load current harmonic decomposition.

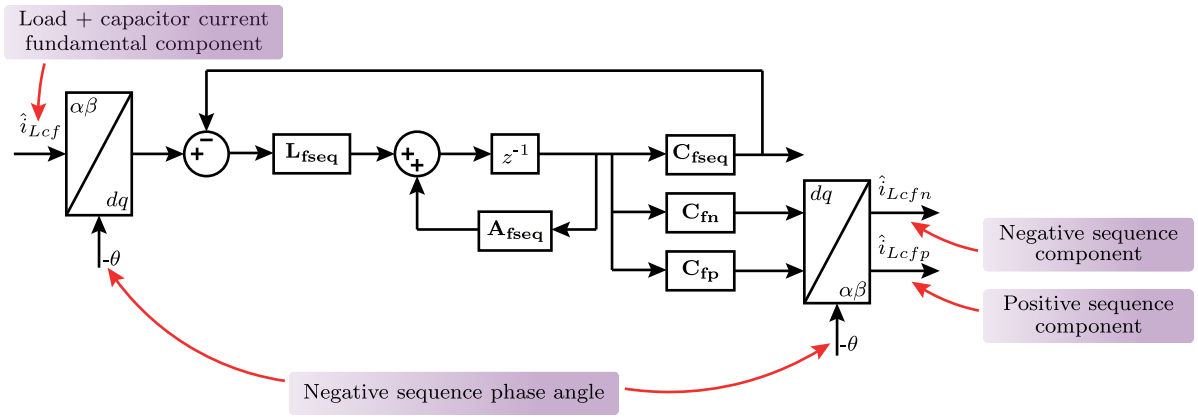


Fig. 5.8. Parallel converter - Load current sequence decomposition.

The estimation error of the current is used as a feedback term for $h_{\alpha\beta}[k] = \mathbf{L_{iLc}}\left(i_{Lc\alpha\beta}[k] - \hat{i}_{Lc\alpha\beta}[k]\right)$, where the feedback gain is obtained using the LQR algorithm, where $\mathbf{L_{iLc}^T} = \text{LQR}(\mathbf{A_{iLc}^T}, \mathbf{C_{iLc}^T}, \mathbf{Q}, \mathbf{R})$. The matrices $\mathbf{Q}$ and $\mathbf{R}$ correspond to the design matrices. The harmonic current decomposition system is shown in Fig. 5.7.

5.2.5 Load current sequence decomposition

Depending on the operating conditions, the fundamental component of the estimated load and capacitor current can be composed of a positive and negative sequence. Assuming that $\hat{i}_{Lcf\alpha\beta}[k]$ is purely fundamental, a DC component plus a second harmonic is obtained after applying the Park transformation synchronized with the grid angle. Both components can be isolated.

Following the idea of the oscillator generator, a system composed of an integrator plus a second harmonic generator is employed.

$$\rho_{dq}[k+1] = \mathbf{A_{fseq}}\rho_{dq}[k] + h_{dq}[k] \tag{5.2.24}$$

$$\mathbf{A_{fseq}} = \begin{bmatrix} \mathbf{I} & \mathbf{O_{2x4}} \\ \mathbf{O_{4x2}} & \mathbf{A_{r2}} \end{bmatrix} \tag{5.2.25}$$

where the negative and positive sequences in dq coordinates are obtained as follows.

$$\hat{i}_{Lcndq}[k] = \underbrace{[\mathbf{I}\ \mathbf{O_{2x4}}]}_{\mathbf{C_{fn}}} \rho_{dq}[k] \tag{5.2.26a}$$

$$\hat{i}_{Lcpdq}[k] = \underbrace{[\mathbf{O}\ \mathbf{C_{r2}}]}_{\mathbf{C_{fp}}} \rho^{dq}[k] \tag{5.2.26b}$$

The total current in dq coordinates is given by the following equations.

$$\hat{i}_{Lcpndq}[k] = \mathbf{C_{seq}} \rho_{dq}[k] \tag{5.2.27a}$$

$$\mathbf{C_{seq}} = \mathbf{C_{fp}} + \mathbf{C_{fn}} \tag{5.2.27b}$$

The correction term of (5.2.24) is generated using the error of the current estimation, $h_{dq}[k] = \mathbf{L_{fseq}}(\hat{i}_{Lcfdq}[k] - \hat{i}_{Lcpndq}[k])$. The feedback gain, $\mathbf{L_{fseq}}$, is designed using the LQR algorithm, where $\mathbf{L^T_{fseq}} = \text{LQR}(\mathbf{A^T_{fseq}}, \mathbf{C^T_{seq}}, \mathbf{Q}, \mathbf{R})$. The matrices $\mathbf{Q}$ and $\mathbf{R}$ correspond to the design matrices. The sequence decomposition of the load current is shown in Fig. 5.8.

5.3 Simulation results

Results of the HDT operating in an MV/LV distribution grid can be found in **Appendix C**. These results take into consideration the distributed parameters of the distribution line.

The simulation results of the HDT based on the experimental setup parameters are presented in this section. The grid and HDT parameters of Table 5.1, and the control parameters presented in Table 5.2, Table 5.3, Table 5.4, Table 5.5, Table 5.6, Table 5.7, Table 5.8 Table 5.9, and Table 5.10. The control system uses a double update PWM, with a switching frequency of 31.25kHz, and min-max modulation. For the parallel converter, the resonant terms, and harmonics estimator are tuned to the harmonics number 1, 3, 5, 7, 11, 13, 17, and 19. On the other side, the series converter controllers are tuned only to the harmonics number 1, 5, and 7.

Table 5.1. Simulation / Experimental parameters

Param.	Value	Param.	Value
Grid line / Load line voltage	122V	L_1 L_2	200μH
DC-Link voltage	250V	C_1 C_2	12.6μF
L_g - R_g	550μH - 1[Ω]	N_{se}	1/5
C_{dc}	6400μF	h	16μs

Table 5.2. Series converter - State feedback parameters

State feedback parameters							
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**	**Param.**	**Value**
$\mathbf{L_g}(1)$	1.459**I**	$\mathbf{L_g}(2)$	13.82**I**	$\mathbf{L_g}(3)$	0.53**I**	$\mathbf{L_g}(4)$	-78.56**I**
$\mathbf{L_g}(5)$	3.473**I**	$\mathbf{L_g}(6)$	468.82**I**	$\mathbf{L_g}(7)$	1.06**I**	$\mathbf{L_g}(8)$	1147.7**I**
$\mathbf{L_g}(9)$	0.9696**I**	—	—	—	—	—	—

Table 5.3. Series converter - Resonant terms

Resonant terms parameters			
Param.	**Value**	**Param.**	**Value**
$\mathbf{A_{r1}}$	$\begin{bmatrix} 1 & 1.6\text{e-}5 \\ -1.5791 & 1 \end{bmatrix}$	$\mathbf{A_{r5}}$	$\begin{bmatrix} 0.9996 & 1.599\text{e-}5 \\ -39.474 & 0.9997 \end{bmatrix}$
$\mathbf{A_{r7}}$	$\begin{bmatrix} 0.994 & 1.599\text{e-}5 \\ -77.3617 & 0.9994 \end{bmatrix}$	—	—
$\mathbf{B_{r1}}$	$\begin{bmatrix} 1.28\text{e-}6 \\ 0.16 \end{bmatrix}$	$\mathbf{B_{r5}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.16 \end{bmatrix}$
$\mathbf{B_{r7}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.16 \end{bmatrix}$	—	—

Table 5.4. Series converter - Capacitor voltage observer

Capacitor voltage estimator			
Param.	**Value**	**Param.**	**Value**
$\mathbf{L_{v1}}(1)$	0.61**I**	$\mathbf{L_{v1}}(2)$	0.614**I**

Table 5.5. Series converter - Grid voltage observer

Grid voltage estimator parameters					
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**
$\mathbf{L_g}(1)$	0.655**I**	$\mathbf{L_g}(2)$	-0.6065**I**	$\mathbf{L_g}(3)$	-0.402**I**
$\mathbf{L_g}(4)$	-142.62**I**	$\mathbf{L_g}(5)$	-0.465**I**	$\mathbf{L_g}(6)$	-5.5**I**

Table 5.6. Parallel converter - State feedback parameters

State feedback parameters							
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**	**Param.**	**Value**
$\mathbf{K_2}(1)$	3.29**I**	$\mathbf{K_2}(2)$	-2.05**I**	$\mathbf{K_2}(3)$	-0.28**I**	$\mathbf{K_2}(4)$	0.12**I**
$\mathbf{K_2}(5)$	-11.94**I**	$\mathbf{K_2}(6)$	0.53**I**	$\mathbf{K_2}(7)$	80.02**I**	$\mathbf{K_2}(8)$	0.13**I**
$\mathbf{K_2}(9)$	90.76**I**	$\mathbf{K_2}(10)$	0.1492**I**	$\mathbf{K_2}(11)$	132.6**I**	$\mathbf{K_2}(12)$	0.14**I**
$\mathbf{K_2}(13)$	-195.2**I**	$\mathbf{K_2}(14)$	0.15**I**	$\mathbf{K_2}(15)$	-89.06**I**	$\mathbf{K_2}(16)$	0.16**I**
$\mathbf{K_2}(17)$	-515.4**I**	$\mathbf{K_2}(18)$	0.12**I**	$\mathbf{K_2}(19)$	-387.5**I**	$\mathbf{K_2}(20)$	0.15**I**

Table 5.7. Parallel converter - Resonant terms

Resonant terms parameters			
Param.	**Value**	**Param.**	**Value**
$\mathbf{A_{r1}}$	$\begin{bmatrix} 1 & 1.6\text{e-}5 \\ -1.5791 & 1 \end{bmatrix}$	$\mathbf{A_{r3}}$	$\begin{bmatrix} 0.9998 & 1.599\text{e-}5 \\ -14.211 & 0.9998 \end{bmatrix}$
$\mathbf{A_{r5}}$	$\begin{bmatrix} 0.9996 & 1.599\text{e-}5 \\ -39.474 & 0.9997 \end{bmatrix}$	$\mathbf{A_{r7}}$	$\begin{bmatrix} 0.994 & 1.599\text{e-}5 \\ -77.3617 & 0.9994 \end{bmatrix}$
$\mathbf{A_{r11}}$	$\begin{bmatrix} 0.9985 & 1.599\text{e-}5 \\ -190.97 & 0.9985 \end{bmatrix}$	$\mathbf{A_{r13}}$	$\begin{bmatrix} 0.997 & 1.598\text{e-}5 \\ -266.684 & 0.9979 \end{bmatrix}$
$\mathbf{A_{r17}}$	$\begin{bmatrix} 0.996 & 1.598\text{e-}5 \\ -455.81 & 0.9964 \end{bmatrix}$	$\mathbf{A_{r19}}$	$\begin{bmatrix} 0.995 & 1.597\text{e-}5 \\ -569.202 & 0.995 \end{bmatrix}$
$\mathbf{B_{r1}}$	$\begin{bmatrix} 1.28\text{e-}6 \\ 0.16 \end{bmatrix}$	$\mathbf{B_{r3}}$	$\begin{bmatrix} 1.28\text{e-}6 \\ 0.16 \end{bmatrix}$
$\mathbf{B_{r5}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.16 \end{bmatrix}$	$\mathbf{B_{r7}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.16 \end{bmatrix}$
$\mathbf{B_{r11}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.15 \end{bmatrix}$	$\mathbf{B_{r13}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.159 \end{bmatrix}$
$\mathbf{B_{r17}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.159 \end{bmatrix}$	$\mathbf{B_{r19}}$	$\begin{bmatrix} 1.279\text{e-}6 \\ 0.159 \end{bmatrix}$

Table 5.8. Parallel converter - Load harmonic estimator

Harmonic estimator parameters			
Param.	**Value**	**Param.**	**Value**
$\mathbf{A_{iLc1}}$	$\begin{bmatrix} 1 & 1.6\text{e-}5 \\ -1.5791 & 1 \end{bmatrix}$	$\mathbf{A_{iLc3}}$	$\begin{bmatrix} 0.9998 & 1.599\text{e-}5 \\ -14.211 & 0.9998 \end{bmatrix}$
$\mathbf{A_{iLc5}}$	$\begin{bmatrix} 0.9996 & 1.599\text{e-}5 \\ -39.474 & 0.9997 \end{bmatrix}$	$\mathbf{A_{iLc7}}$	$\begin{bmatrix} 0.994 & 1.599\text{e-}5 \\ -77.3617 & 0.9994 \end{bmatrix}$
$\mathbf{A_{iLc11}}$	$\begin{bmatrix} 0.9985 & 1.599\text{e-}5 \\ -190.97 & 0.9985 \end{bmatrix}$	$\mathbf{A_{iLc13}}$	$\begin{bmatrix} 0.997 & 1.598\text{e-}5 \\ -266.684 & 0.9979 \end{bmatrix}$
$\mathbf{A_{iLc17}}$	$\begin{bmatrix} 0.996 & 1.598\text{e-}5 \\ -455.81 & 0.9964 \end{bmatrix}$	$\mathbf{A_{iLc19}}$	$\begin{bmatrix} 0.995 & 1.597\text{e-}5 \\ -569.202 & 0.995 \end{bmatrix}$
$\mathbf{L_{iLc1}}$	$\begin{bmatrix} 1.28\text{e-}6 & 0.16 \end{bmatrix}$	$\mathbf{L_{iLc3}}$	$\begin{bmatrix} 1.28\text{e-}6 & 0.16 \end{bmatrix}$
$\mathbf{L_{iLc5}}$	$\begin{bmatrix} 1.279\text{e-}6 & 0.16 \end{bmatrix}$	$\mathbf{L_{iLc7}}$	$\begin{bmatrix} 1.279\text{e-}6 & 0.16 \end{bmatrix}$
$\mathbf{L_{iLc11}}$	$\begin{bmatrix} 1.279\text{e-}6 & 0.15 \end{bmatrix}$	$\mathbf{L_{iLc13}}$	$\begin{bmatrix} 1.279\text{e-}6 & 0.159 \end{bmatrix}$
$\mathbf{L_{iLc17}}$	$\begin{bmatrix} 1.279\text{e-}6 & 0.159 \end{bmatrix}$	$\mathbf{L_{iLc19}}$	$\begin{bmatrix} 1.279\text{e-}6 & 0.159 \end{bmatrix}$

Table 5.9. Parallel converter - Load harmonic estimator

Sequence decomposition parameters			
Param.	**Value**	**Param.**	**Value**
$\mathbf{A_{fseq2}}$	$\begin{bmatrix} 0.999 & 1.6\text{e-}5 \\ -6.3164 & 0.999 \end{bmatrix}$	$\mathbf{A_{fseq0}}$	1
$\mathbf{L_{fseq2}}$	$\begin{bmatrix} 0.8961 & 254.34 \end{bmatrix}$	$\mathbf{L_{fseq0}}$	0.0983

Table 5.10. Parallel converter - DC-Link controller

DC-Link controller					
Param.	**Value**	**Param.**	**Value**	**Param.**	**Value**
K_{vdci}	0.000291	K_{vdcp}	0.3272	-	-
$K_{notch11}$	0.9989	$K_{notch12}$	-6.313	$K_{notch13}$	1.599e-5
$K_{notch21}$	0.0000159	$K_{notch22}$	0.9994	$K_{notch23}$	1.279e-10
$K_{notch31}$	-62.79	$K_{notch32}$	1.9833	$K_{notch33}$	0.9949

5.3.1 Parameter stability analysis

The stability of the HDT is assessed using the complete state-space representation of the HDT, as follows.

$$x_{12\alpha\beta}[k+1] = \mathbf{A_{12}} x_{12\alpha\beta}[k] + \begin{bmatrix} \mathbf{B_{1er}} \\ \mathbf{O} \end{bmatrix} i^*_{2\alpha\beta}[k] + \begin{bmatrix} \mathbf{O} \\ \mathbf{B_{2er}} \end{bmatrix} v^*_{1\alpha\beta}[k] \tag{5.3.1a}$$

$$\mathbf{A_{12}} = \begin{bmatrix} \mathbf{A_{1er}} - \mathbf{B_{1er}}\mathbf{K_1} & \mathbf{P_{1er}}\mathbf{C_{2er}} \\ \mathbf{P_{2er}}\mathbf{C_{1er}} & \mathbf{A_{2er}} - \mathbf{B_{2er}}\mathbf{K_2} \end{bmatrix} \tag{5.3.1b}$$

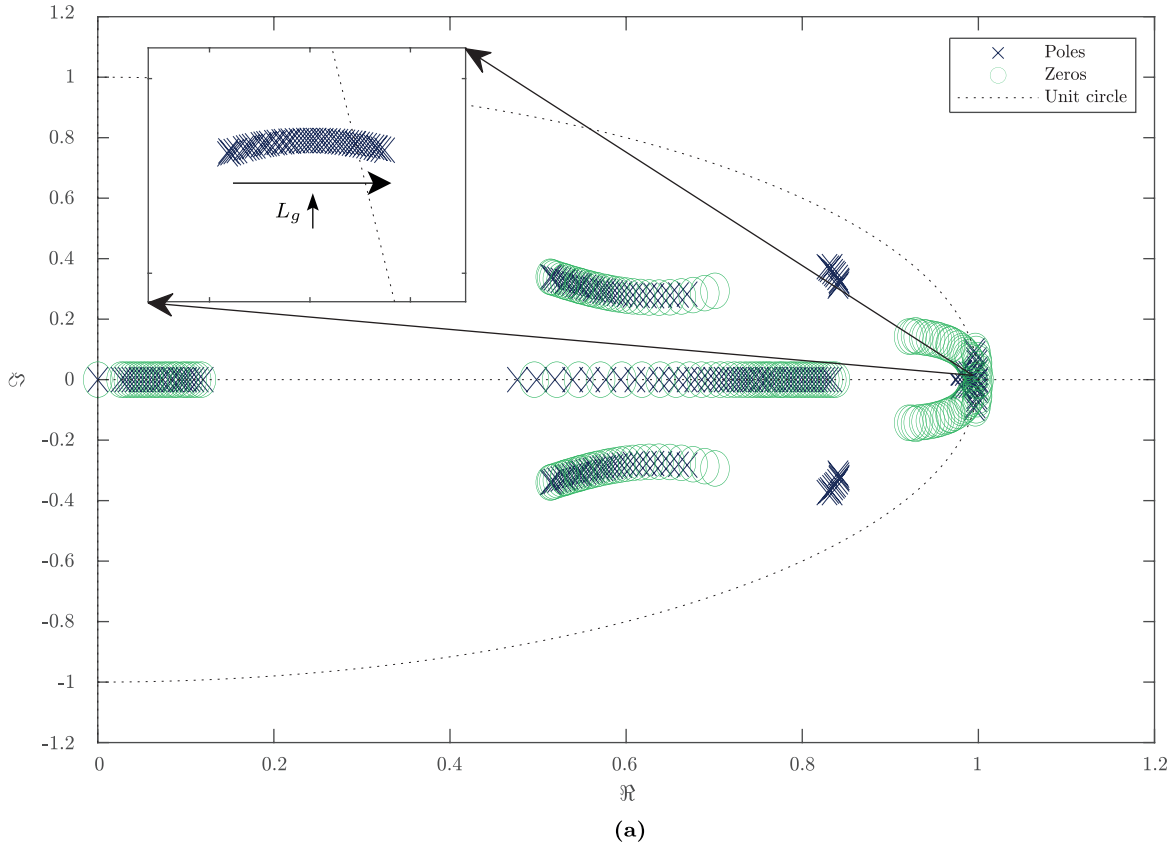
The poles of the system are given by $\det((z\mathbf{I} - \mathbf{A_{12}})) = 0$, and its root locus is plotted in Fig. 5.9(a) based on the parameters of Table Table 5.1 for different values of grid inductance. The results show that the stability is lost when the grid inductance reaches 2mH, four times the value considered for the design.

Fig. 5.9(b) shows the root locus for different values of the parallel resistance of capacitor C_2, which can be used to model a resistive load. Negative values are also considered in order to emulate a regenerative load. For the HDT under simulation, the limit is found at -6.8Ω. In order to enable the operation of the HDT under higher regeneration conditions, a change in the control gains would be required. Nonetheless, that is out of the scope of this article.

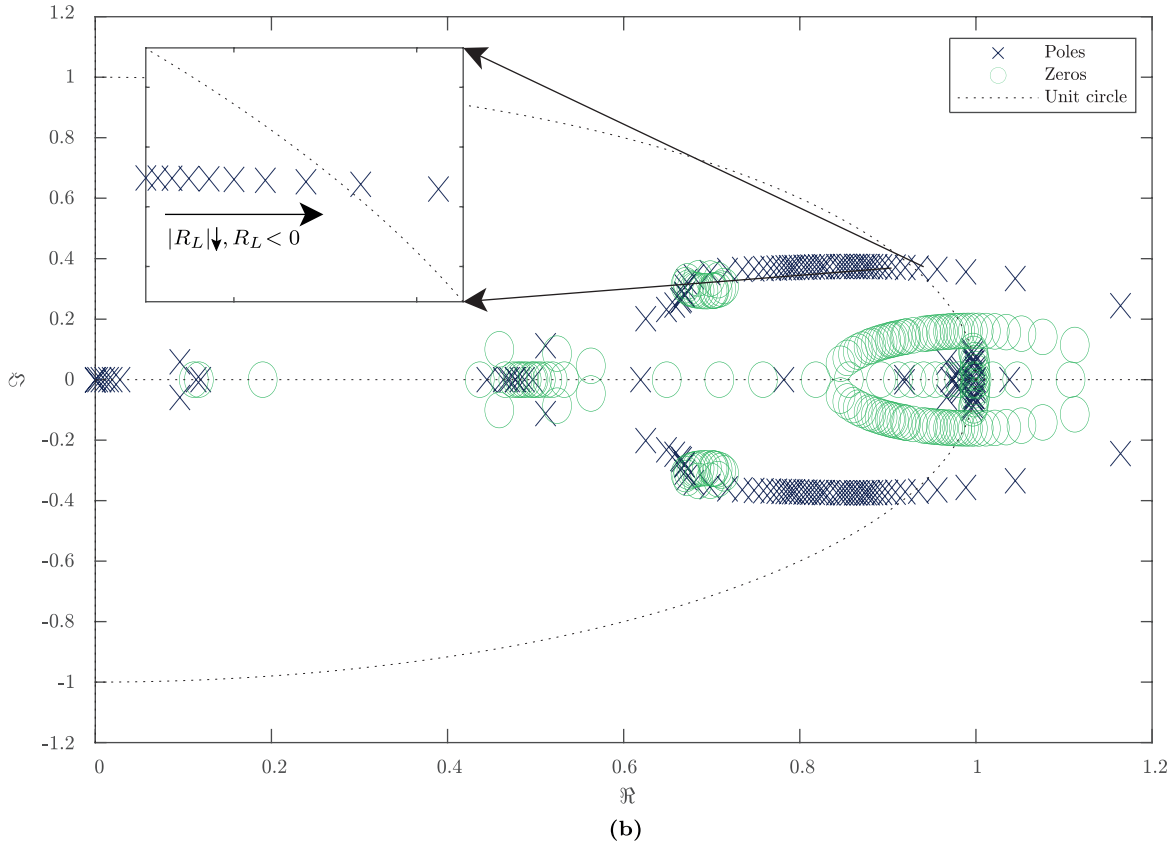
5.3.2 Simulation cases

Three cases are presented in Fig. 5.10, which correspond to the HDT under a balanced sag, a distorted grid, and an active distribution grid producing a reverse power flow.

In the first case, a voltage sag is applied at $t = 60$ms which is correctly compensated, keeping the secondary side voltage to its nominal amplitude. This operation takes approximately one cycle. At the same time, the parallel converter compensates for the load harmonics, improving the quality of the secondary side current. During the sag compensation, it can be seen that the secondary-side current increases due to the effect of the circulating active power flow [38]. A load step is applied at $t = 100$ms, showing the correct operation of the parallel converter. Due to the grid impedances, the load change disturbs the amplitude of the grid voltage, which is also compensated by the series converter. At $t = 140$ms the grid voltage is set back to its initial value, but due to the load change, there grid voltage amplitude is over its nominal value, which is compensated



(a)



(b)

Fig. 5.9. Root locus: **(a)** L_g from 550μH to 11mH. **(b)** Load resistance from 110Ω to -110Ω.

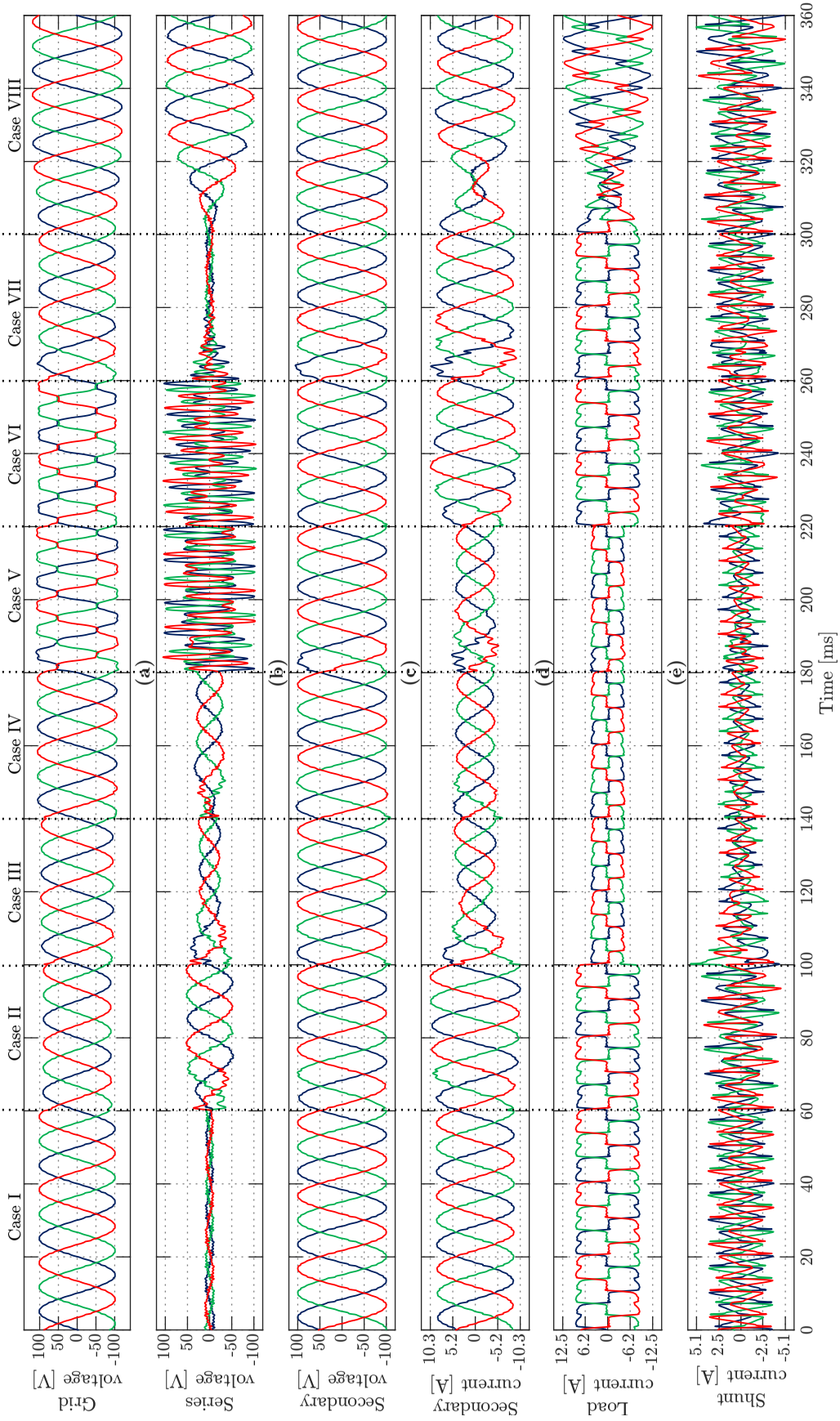


Fig. 5.10. Simulations results under a voltage sag, distorted grid and reverse power flow. **(a)** Grid voltage. **(b)** Series voltage. **(c)** Secondary-side voltage. **(d)** Secondary-side current. **(e)** Load current. **(f)** parallel converter current.

Table 5.11. Simulation cases - THD values

	THD [%]			
Cases	**Grid voltage**	**Load voltage**	**Load current**	**Secondary current**
I	0.12	0.14	26.6	0.2
II	0.14	0.14	26.6	0.2
III	1.1	1.2	27.5	3.3
IV	0.9	1.2	27.5	3.7
V	13.4	1.2	27.5	3.5
VI	14	1.4	26.6	2.4
VII	1.2	1.4	26.6	2.4
VIII	1.1	1.5	21.5	2.2

by the series converter.

Then, the grid voltage is polluted with 10% of 5th and 7th harmonics $t = 180$ms. The resonant controllers of the series converter mitigate them and improve the voltage on the secondary side. Additionally, the load is increased to its original value at $t = 220$ms, stabilizing the secondary side current in about a cycle. This time involves the controller dynamics and the load harmonics decomposition. Additionally, it can be seen that voltage on the secondary side presents slight high-frequency distortion, which comes from the uncompensated high-frequency components of the secondary side currents that flow through the leakage impedance of the LFT. At $t = 260$ms the grid voltage distortion is cleared.

In the last cases, the nonlinear load is kept and the renewable generation is activated at $t = 300$ms reversing the power flow through the HDT. It can be seen that during the power flow reversal, the grid voltage increases due to the interaction between the injected current and the grid impedance. Nonetheless, the series converter injects the complementary voltage, compensating the voltage swell, and maintaining the secondary side voltage regulated.

Table 5.11 shows the THD values of the grid and secondary voltage, and load and secondary current for each case of Fig. 5.10. The secondary voltage and current are highlighted due to they are the control objective and represent the improvement in the load supply and grid current, as well as the operating conditions of the main LFT of the HDT. It can be seen that in the worse operating conditions, cases V and VI, the THD of the load voltage is one order of magnitude lower than the grid. The same occurs with the secondary current, whose THD is one order of magnitude lower than the load.

5.4 Experimental results

In this section, the experimental results of the proposed HDT are presented. The diagram of the experimental setup is shown in Fig. B.5 of the **Appendix B**, and the parameters are listed in Table 5.1.

The experiments are divided as follows:

- 3-wire distribution gridk: The experiments are carried out using an unbalanced load consisting of a three-phase rectified and a resistive load connected between phase a and b. The reference HDT is shown in Fig. 2.1(a).
- 4-wire distribution grid: The experiments are carried out using an unbalanced load consisting of a three-phase rectified and a resistive load connected between phase a and the neutral wire. The reference HDT is shown in Fig. 2.1(b).

In both scenarios, the control algorithm of the HDT is tested under an unbalanced and nonlinear load, and balanced, unbalanced, and polluted grid voltage.

Remark: The experimental results which were included in the derived publication of this chapter were obtained using two oscilloscopes Tektronix MSO58B and MDO34. These results correspond to Fig. 5.11, Fig. 5.13, and Fig. 5.15.

Due to the channel number limitation of the oscilloscope, the remaining experimental results were obtained directly from the microcontroller of both power converters and measurement board. Thus, due to memory restrictions, these results were obtained with an equivalent sampling time of 160μs. These results correspond to Fig. 5.12, Fig. 5.14, Fig. 5.16, Fig. 5.17, Fig. 5.18, Fig. 5.19, Fig. 5.20, and Fig. 5.21.

It is worth mentioning that due to the configuration of the control platform, the load current is not measured directly, and instead the summation of the load current with the capacitor current is shown. On the other side, the load current is directly measured in the results obtained via the oscilloscopes.

5.4.1 3-wire grid

Balanced voltage sag and swell

The dynamic response of the HDT under a 15% voltage sag and 15% voltage swell is presented in Fig. 5.11. The HDT is able to compensate for voltage rapidly, preserving the voltage magnitude on the secondary side. The voltage sag is mitigated in half a cycle, whereas the secondary current is stabilized in approximately one and a half cycles. During the compensation period, the magnitude of the fundamental component of the LFT current increases from 9.5A to 11.2A. Although the load current remains unchanged, the increment in the LFT current occurs due to the circulating active power flow. When the HDT compensates for a voltage sag of 15%, the circulating active power flow is equal to 17.7% of the load active power. On the other hand, during the voltage swell, a reverse active power flow occurs, which decreases the LFT current to 8.2A. This corresponds to a reduction of 13% [96]. The circulating active power flow adds up to the LFT copper losses, which are dependent on the active power of the load and the magnitude of the sag/swell of the grid voltage.

The parallel connected capacitor on the secondary side is the cause of the current peaks presented in the LFT current when the voltage sag or swell is applied. The current peak during the transition from voltage sag to voltage swell is higher because the voltage variation corresponds to 30%. Due to the higher voltage variation, the required time to regulate the secondary voltage increases to one cycle, mainly due to the controller antiwindup. The controller eliminates the effect of the fundamental component of the capacitor current through the reactive power controller. In steady-state, the currents are practically sinusoidal and in phase with the PCC voltage, and only the uncompensated high-frequency components are present. The controller of the parallel converter balances the load, improves the THD, and corrects the power factor.

Unbalanced voltage sag

The results shown in Fig. 5.12 present the response of the HDT while being subject to a sudden grid voltage unbalance, while feeding a nonlinear and unbalanced load. The grid voltage during the disturbance period correspond to a 10% voltage sag on the phases b and c, while the phase a operates at its nominal value.

The results show that the control algorithm of the HDT is able to compensate for the grid voltage unbalanced, providing a sinusoidal and balanced voltage to the loads, as seen in Fig. 5.12(b). For these means, the series converter injects the complementary grid voltages as shown in Fig. 5.12(c). Although the phase a of the grid is supposed to operate

at its nominal value, the current flowing on the line generates an additional voltage drop which is compensated by the series converter, which is observed as a small voltage on the phase a of the series converter in comparison with the remaining phases. Additionally, part of the injected voltage is used to compensate for the internal voltage drops of the transformer.

Finally, there is an increase in the secondary current, or equivalently there is a circulating active power flow, which is due to the equivalent positive sequence disturbance of the grid voltage.

Distorted grid voltage

Results presented in Fig. 5.13 show the behavior of the HDT under a sudden injection of 10% of 5th and 7th harmonic on the grid voltage. Under these conditions, the voltage THD is equal to 14.8%. The voltage disturbance is mitigated in approximately one cycle, whereas the secondary current is stabilized in one and a half cycles. In steady-state, the THD of the secondary voltage is reduced to 0.9%. The effect of the uncompensated harmonics of the load current on the LFT impedance contributes to the distortion on the secondary side. On the other hand, the nonlinear current has a THD of 14.4%, which is then improved to 1.7%. Fig. 5.13(e) presents the harmonic spectrum after the grid distortion is applied. It can be seen that for the secondary current and voltage, the harmonic content is correctly compensated. The harmonics that are left uncompensated, $n > 20$ are present, causing distortion on the waveforms. The transient distortion on the secondary-side current occurs due to the harmonic currents generated by the parallel-connected capacitor when a sudden voltage disturbance is applied. In steady-state, the currents are practically sinusoidal and in phase with the PCC voltage.

The additional results obtained from the microcontrollers of the HDT are shown in Fig. 5.14, in which the voltage of the capacitor of the series converter and the output current of the parallel converter are shown. It can be seen that the series voltage achieves its steady state in one cycle approximately, supplying the harmonic components of the grid voltage. On the other side, the parallel converter current before and after the distortion is practically the same, because a minimal fundamental component is being provided by the series converter, and therefore no additional circulating active power flow is being generated.

Unbalanced and distorted grid voltage

Finally, Fig. 5.15 and Fig. 5.16 show the results when the HDT compensates for an unbalanced and distorted grid voltage. The values of the fundamental and harmonic components of the grid voltage are shown in Table 5.12.

Table 5.12. Values for the unbalanced and distorted grid voltage.

	Phase a	**Phase b**	**Phase c**
Fundamental voltage magnitude	85V	100V	100V
5th harmonic	10%	10%	20%
7th harmonic	10%	10%	20%

The results clearly show how the HDT provides a sinusoidal and balanced voltage on the secondary side while balanced and active currents circulate through the LFT, for which unbalanced and distorted voltages must be supplied by the series converter, as Fig. 5.16(c) shows. Although, not appreciable in the converter current of Fig. 5.16(f), there is a small circulating active power flow due to the balanced component of the grid voltage disturbance. This is observed as a slight increase in the secondary current.

Load steps

The results of Fig. 5.17 show the dynamic response of the HDT for load steps. The operating scenario considers a distorted grid voltage with 10% of 5th and 7th harmonic.

Fig. 5.17(a) shows the transition from no-load to the connection of 6-pulse bridge rectifier at $t = 20$ms. During the no-load period, the parallel converter only compensates for the capacitor current, which is verified by observing that the secondary side current is equal to zero. After connecting the load, the steady state is achieved in approximately one and a half cycles. During this operation, and due to the additional current circulating through the grid, the series converter is perturbed. Nonetheless, this disturbance is rapidly cleared, and the secondary side voltage remains regulated during the whole process. Similarly, Fig. 5.17(b) shows the transition when connecting the unbalanced load between the phases a and b at $t = 20$ms. After connecting the load, the steady state is achieved in approximately one and a half cycles, and also the disturbance on the series converter and secondary voltage are cleared rapidly.

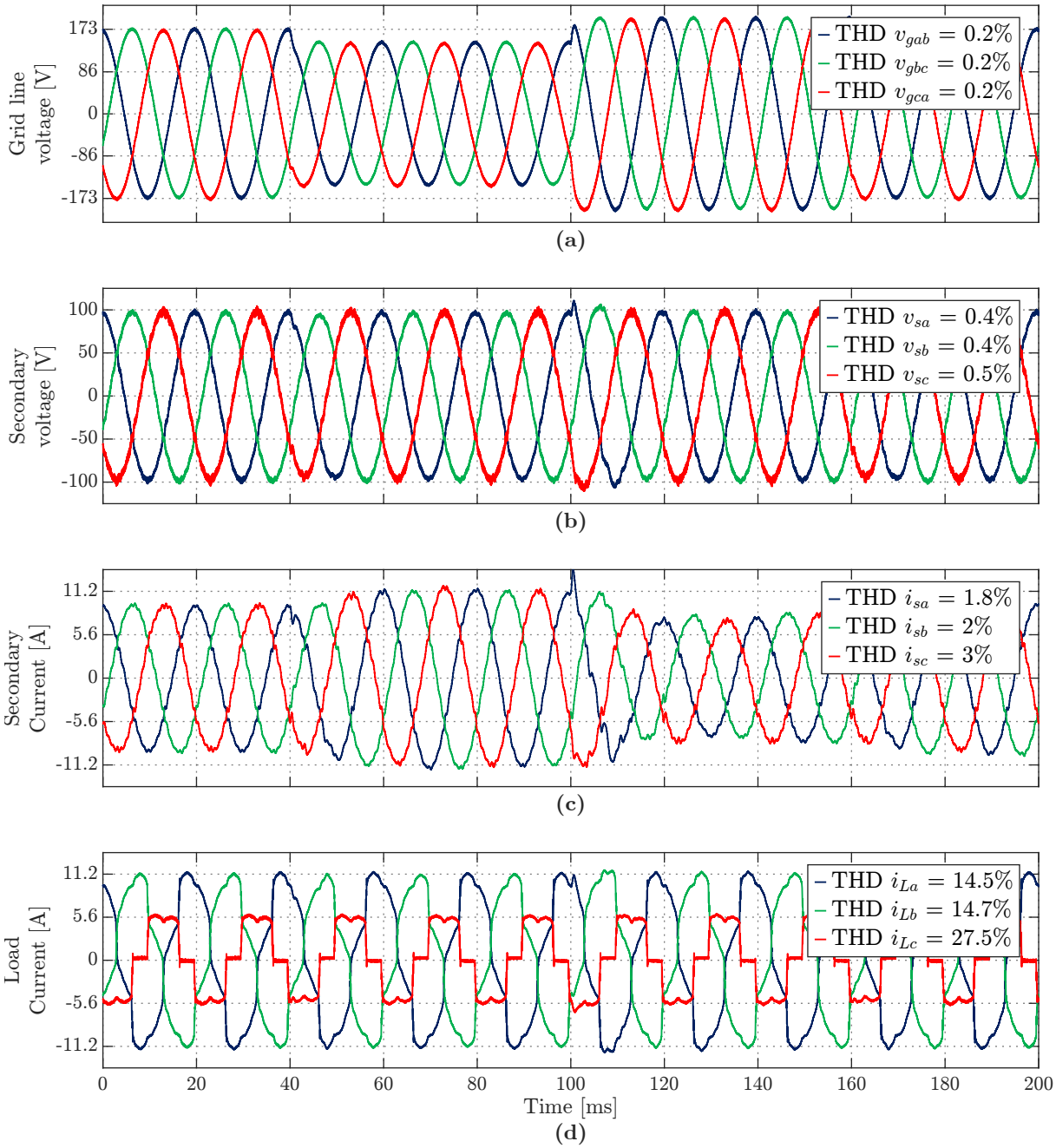


Fig. 5.11. Experimental results - Dynamic response of the HDT under a 15% voltage sag and swell. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Secondary-side current. **(d)** Load current.

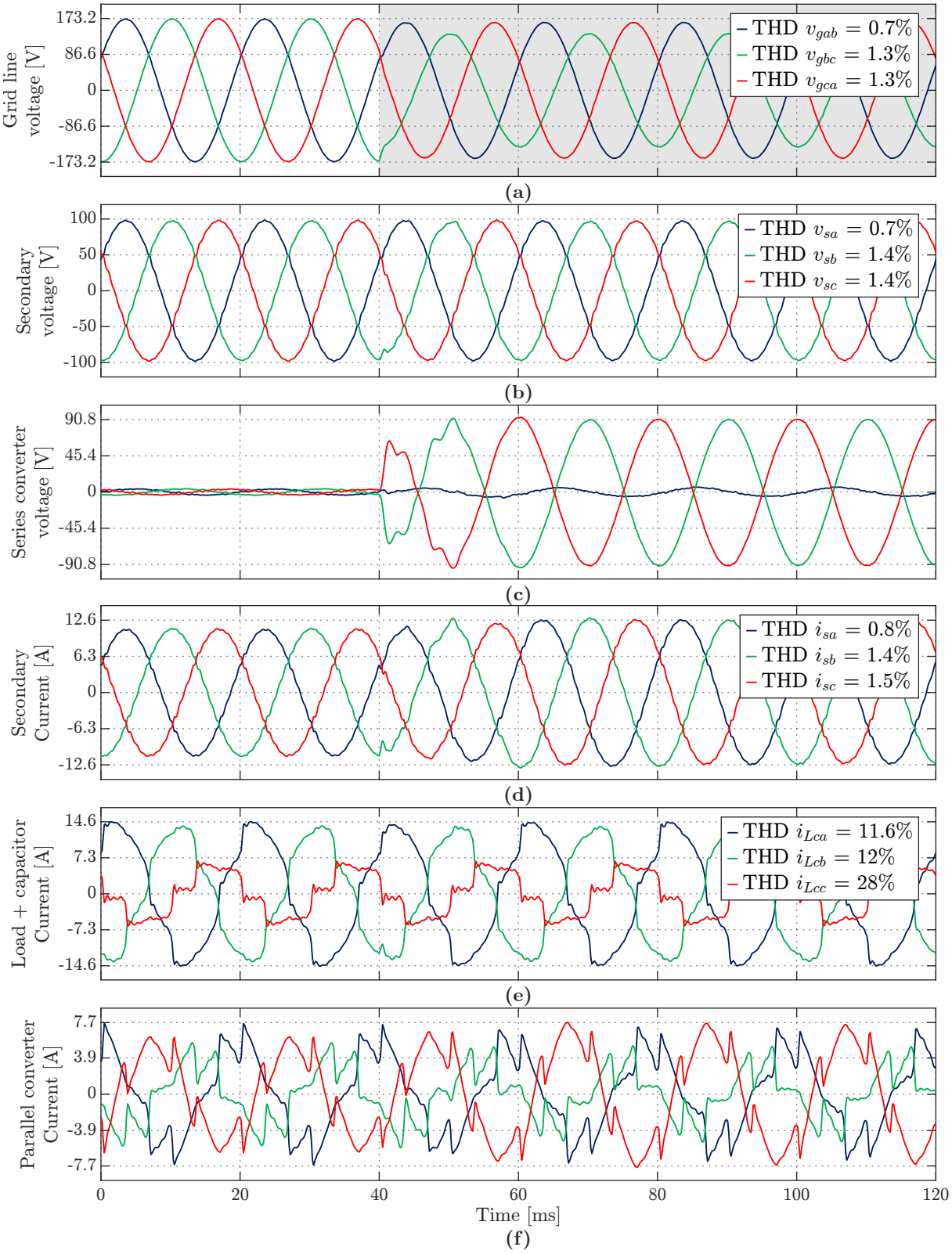


Fig. 5.12. Experimental results (Microcontroller) - Dynamic response of the HDT under an unbalanced grid voltage. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load plus capacitor current. **(f)** Parallel converter current.

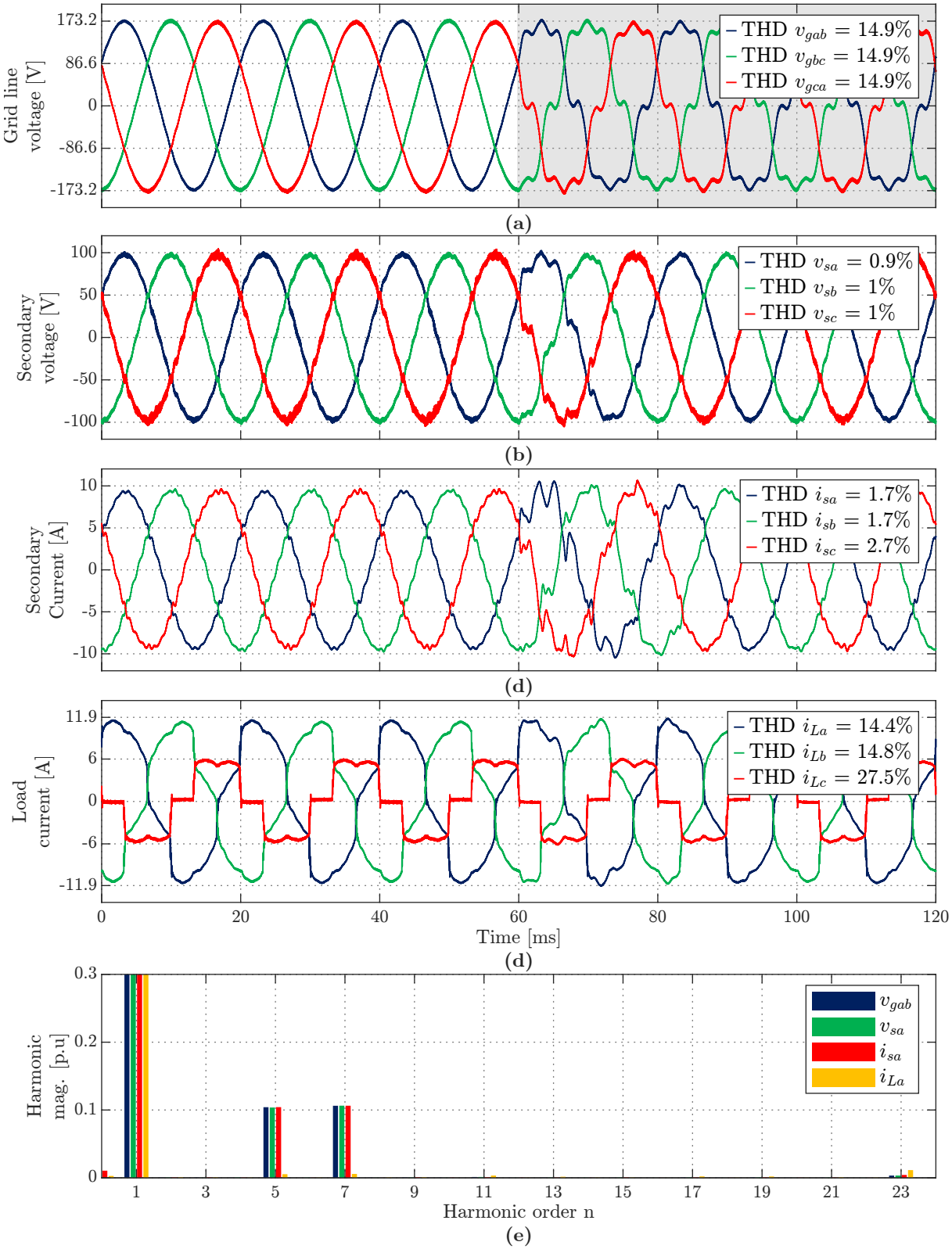


Fig. 5.13. Experimental results - Dynamic response of the HDT under a grid distorted with 10% of 5th and 7th harmonic. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Secondary-side current. **(d)** Load current. **(e)** Normalized FFT during grid distortion (steady state).

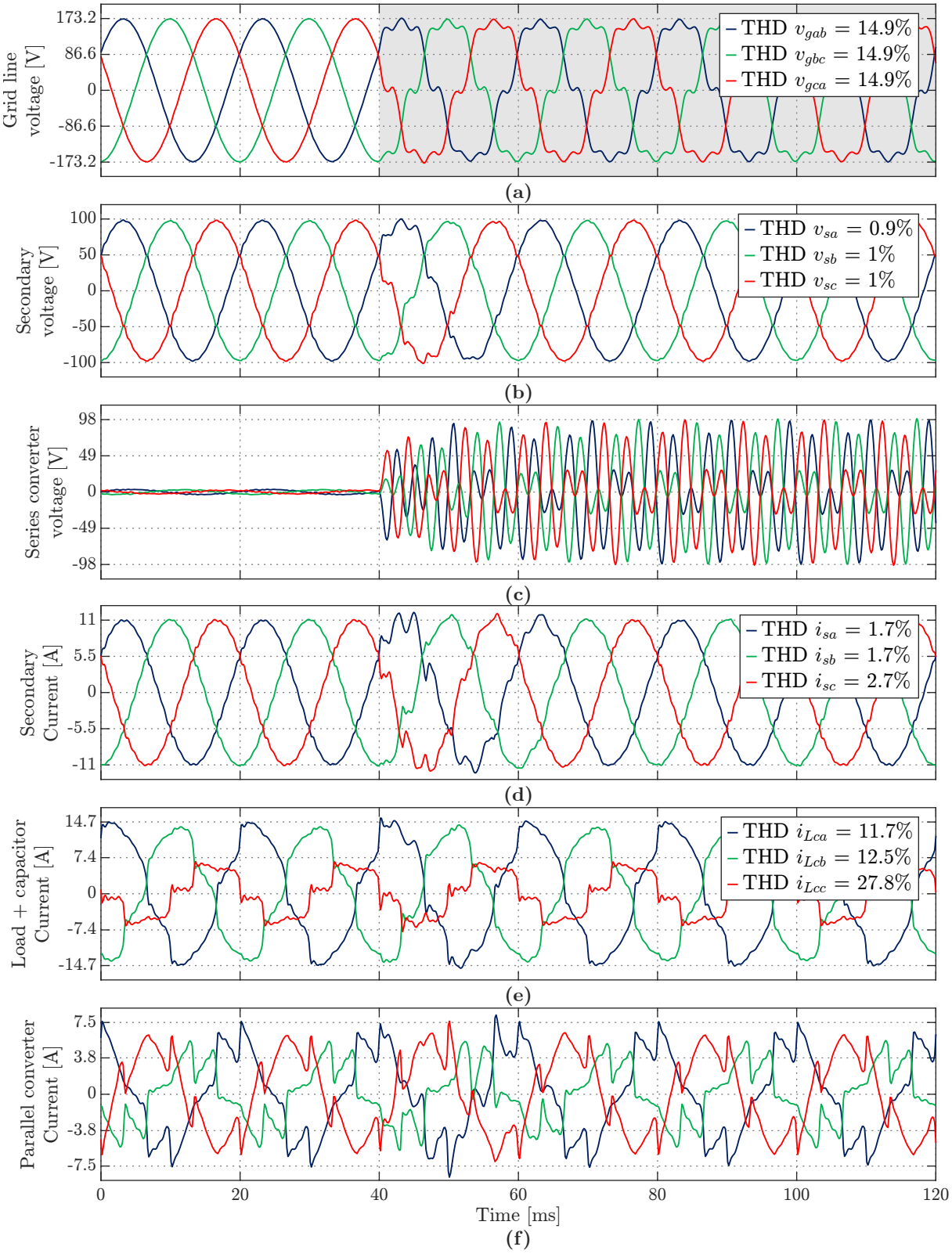


Fig. 5.14. Experimental results (Microcontroller) - Dynamic response of the HDT under a grid voltage distorted with 10% of 5th and 7th harmonic. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load plus capacitor current. **(f)** Parallel converter current.

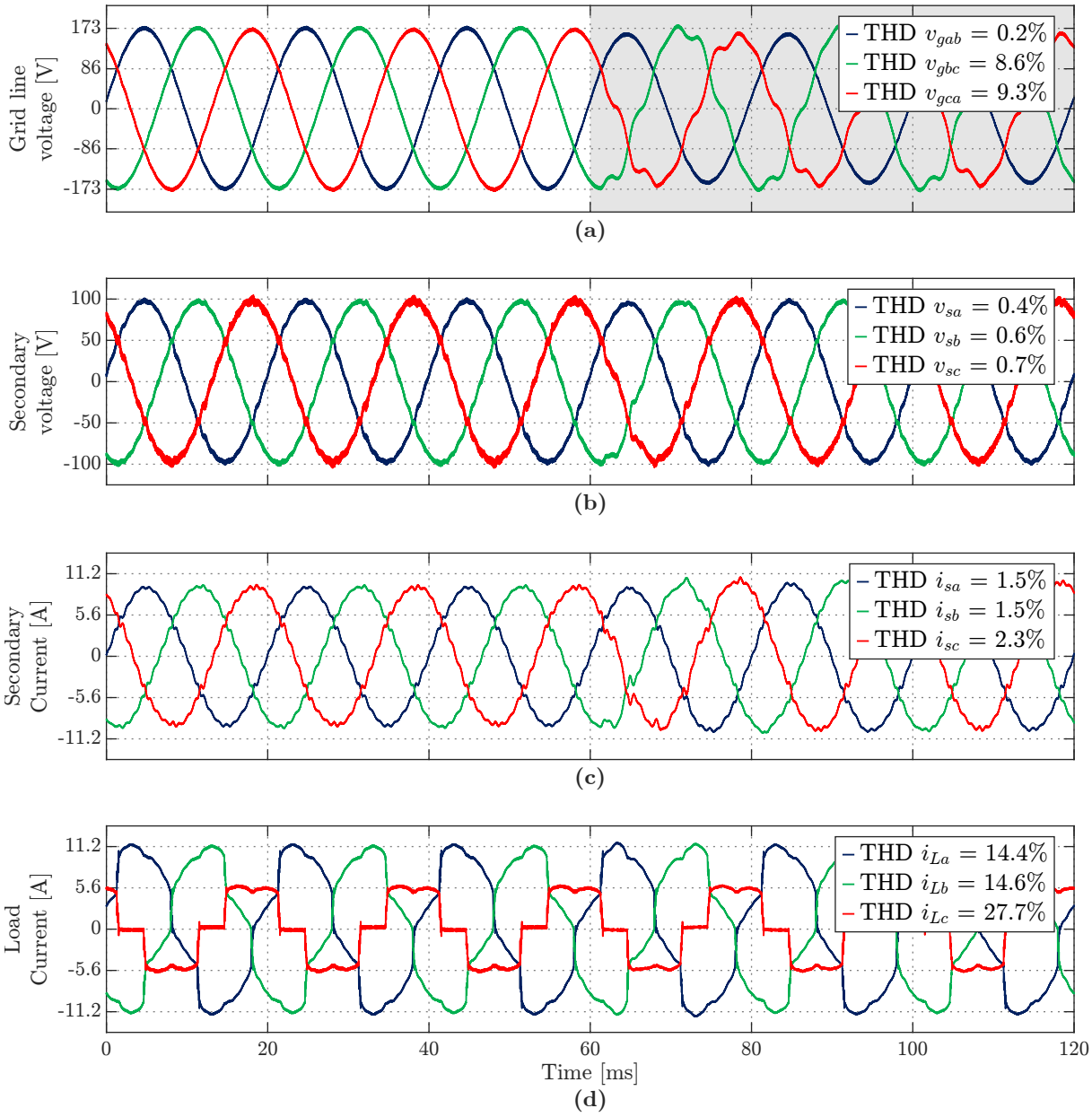


Fig. 5.15. Experimental results - Dynamic response of the HDT under an unbalanced and distorted grid voltage with 5% of 5th and 7th harmonic. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Secondary-side current. **(d)** Load current.

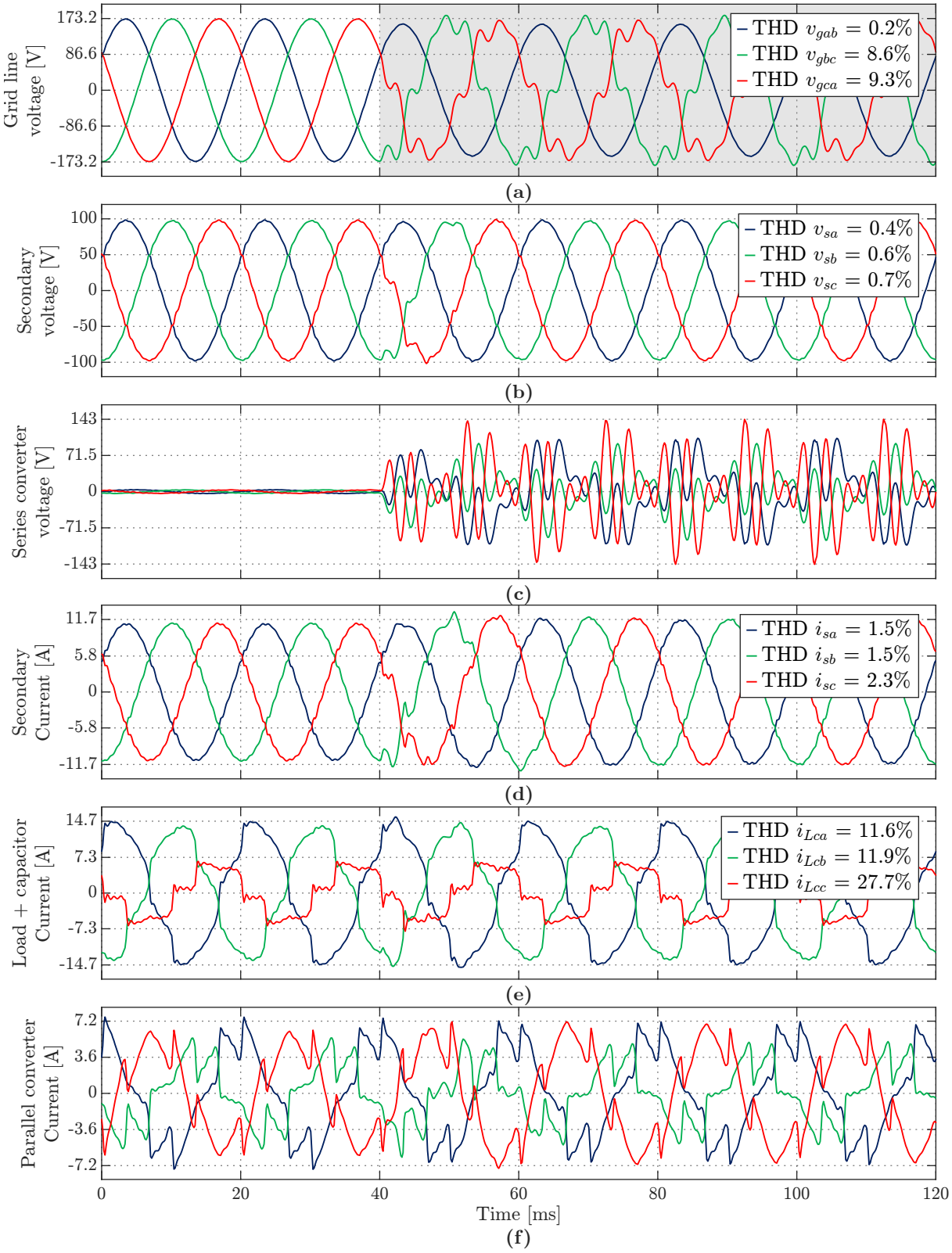


Fig. 5.16. Experimental results (Microcontroller) - Dynamic response of the HDT under an unbalanced and distorted grid voltage with 5% of 5th and 7th harmonic. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load current. **(f)** Parallel converter current.

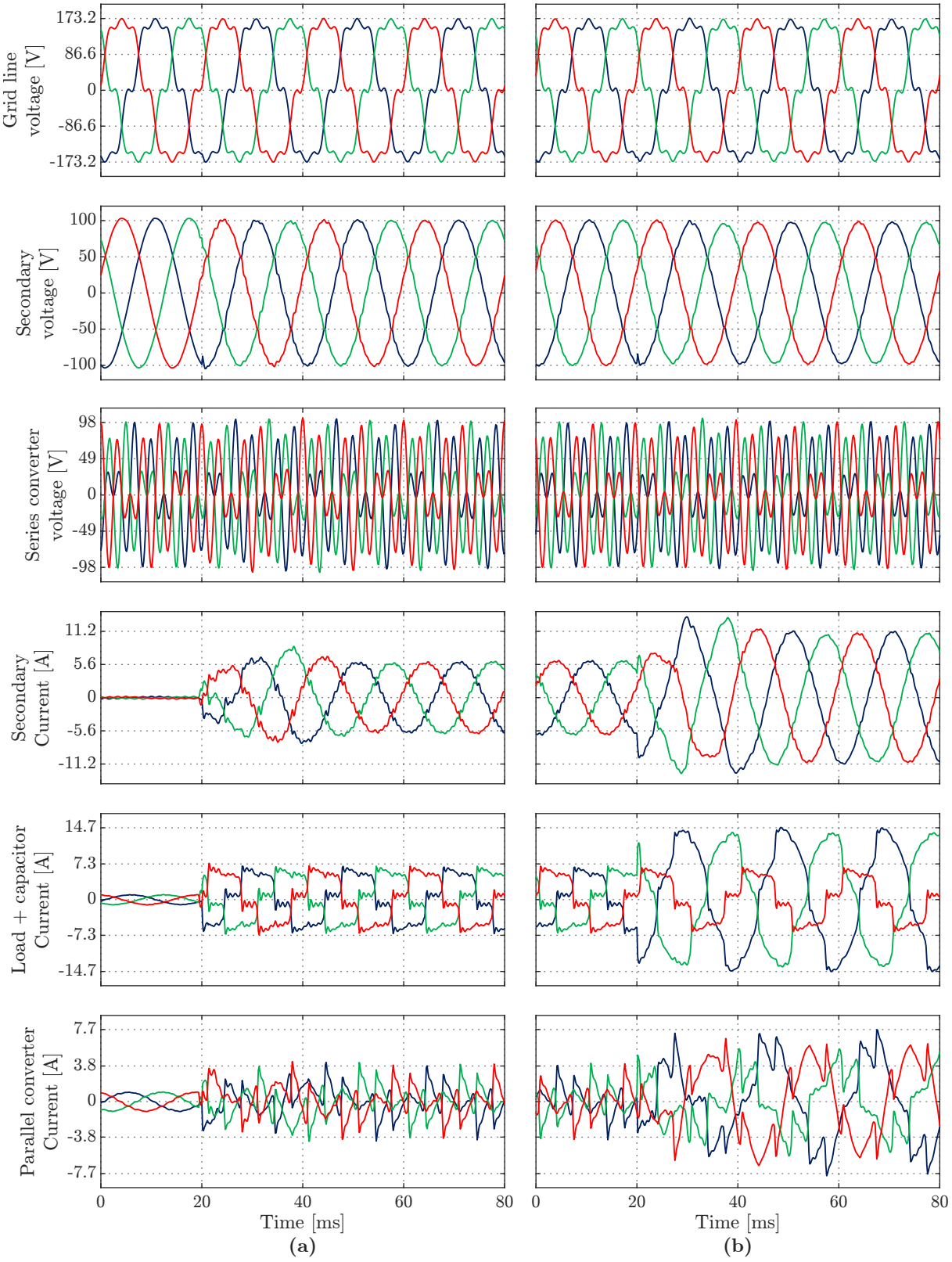


Fig. 5.17. Experimental results (Microcontroller) - Dynamic response of the HDT under a load step with a distorted grid. **(a)** Connecting the 6-pulse bridge rectifier. **(b)** Connecting the resistive load between phases a and b.

5.4.2 4-wire grid

As an extension of the experimental results presented in the previous section, the operation of the HDT considering a 4-wire low voltage grid is presented. The operating conditions are the same as in the previous section, which are summarized as follows:

- Operation under an unbalanced grid voltage: Fig. 5.18.
- Operation under a distorted grid voltage: Fig. 5.19.
- Operation under an unbalanced and distorted grid voltage: Fig. 5.20.
- Neutral-connected load step: Fig. 5.21.

The only difference is that now the resistive load is connected between the phase a and the neutral, generating a common-mode current which now must be compensated by the additional 4th leg of the parallel converter.

The results presented in this section show a correct and stable operation of the HDT in a 4-wire grid. Due to the γ component of the current reference being equal to the γ component of the load current, a fast control is achieved, achieving the steady state in less than half of a cycle. This can be clearly observed while applying the load step, in Fig. 5.21(e).

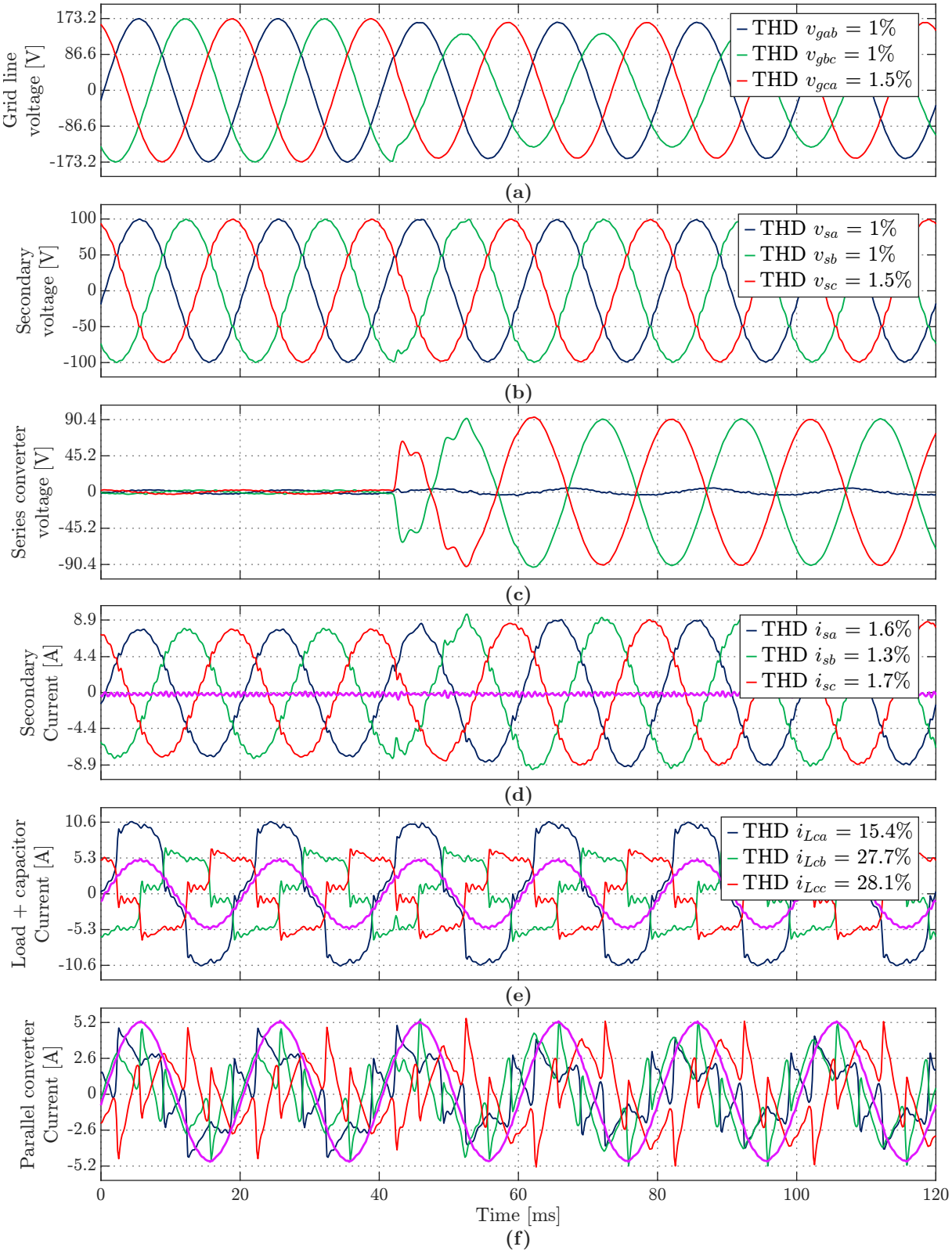


Fig. 5.18. Experimental results (Microcontroller) - 4-wire grid - Dynamic response of the HDT under an unbalanced grid voltage. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load plus capacitor current. **(f)** Parallel converter current.

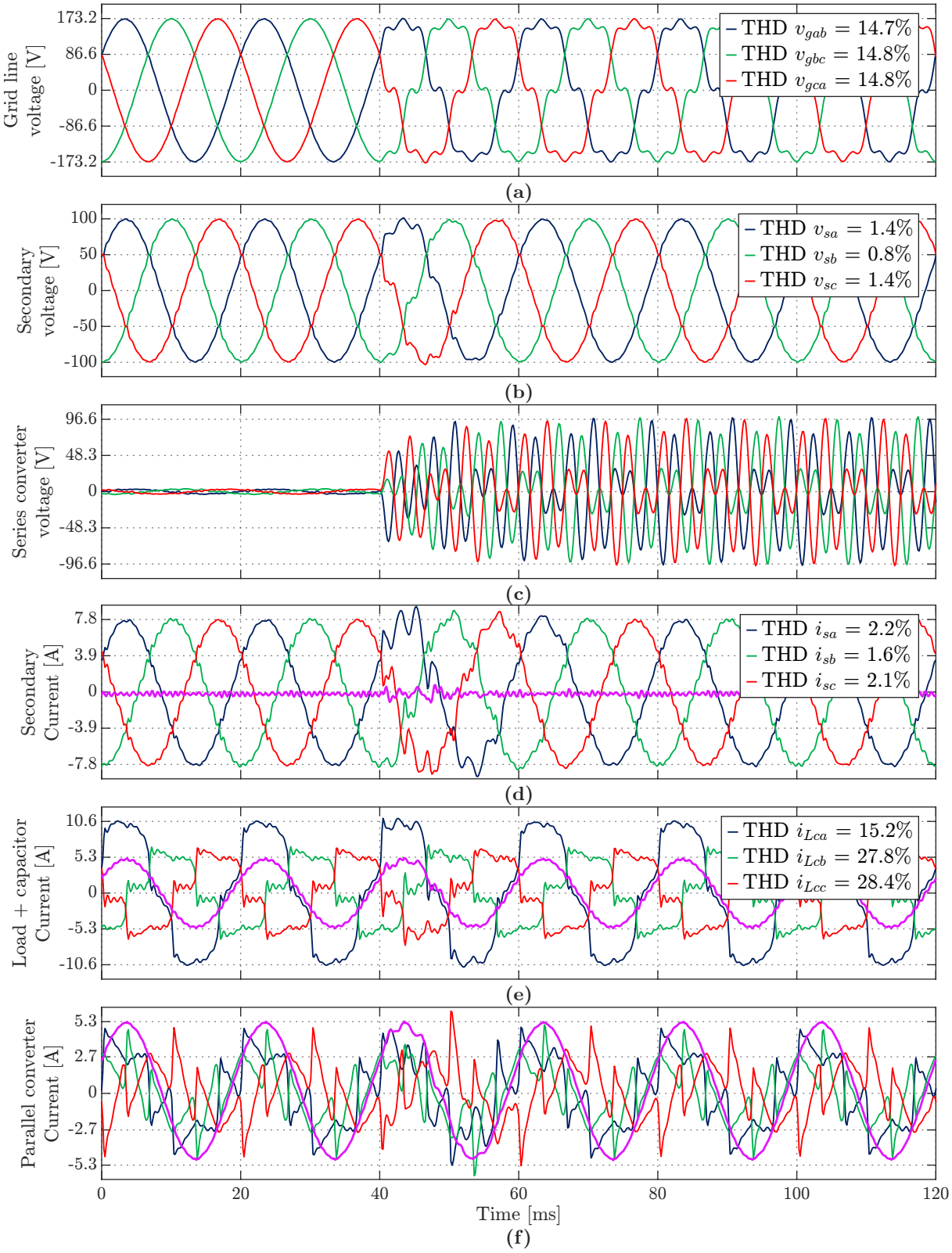


Fig. 5.19. Experimental results (Microcontroller) - 4-wire grid - Dynamic response of the HDT under a grid voltage distorted with 10% of 5th and 7th harmonic. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load plus capacitor current. **(f)** Parallel converter current.

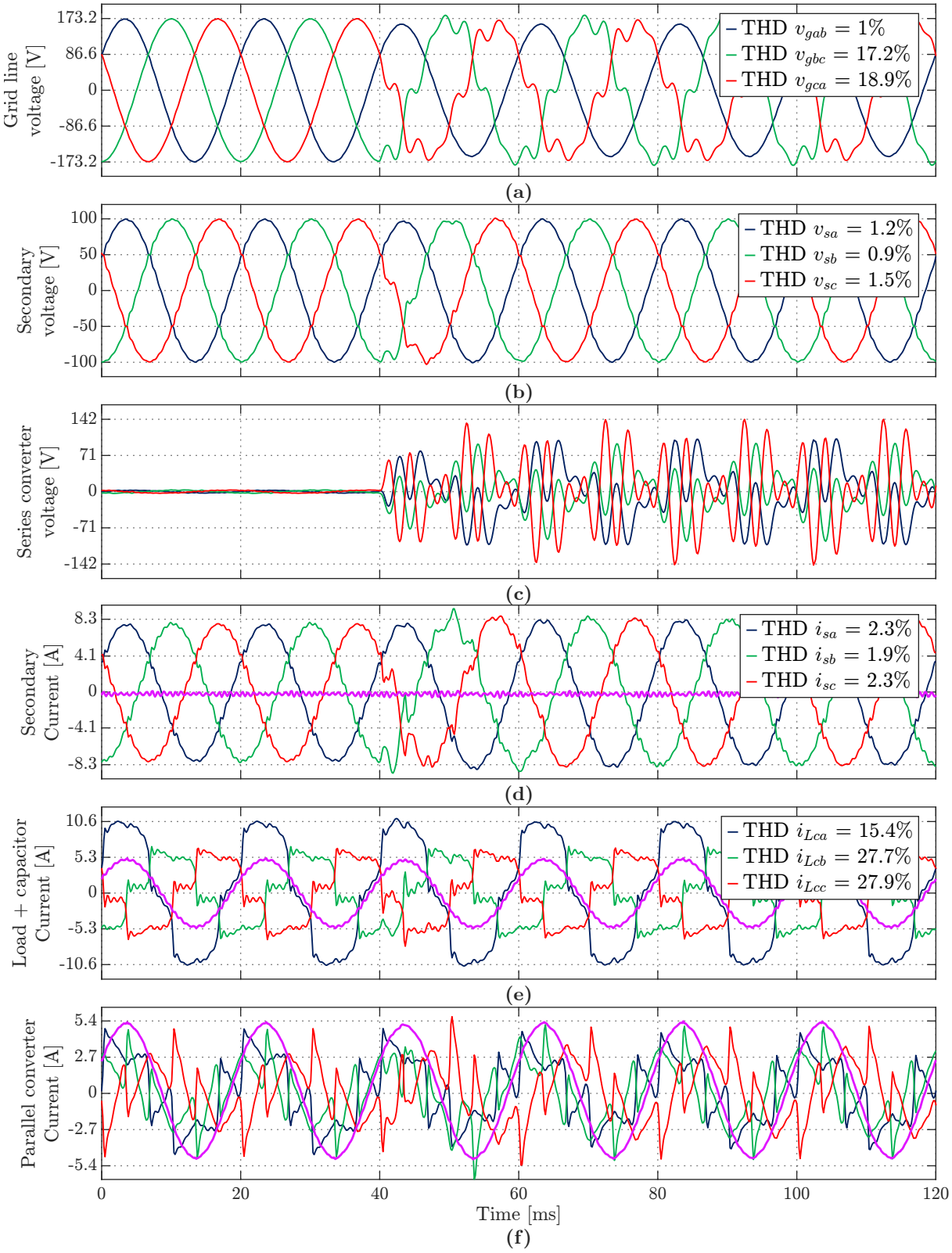


Fig. 5.20. Experimental results (Microcontroller) - 4-wire grid - Dynamic response of the HDT under an unbalanced and distorted grid voltage with 5% of 5th and 7th harmonic. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load current. **(f)** Parallel converter current.

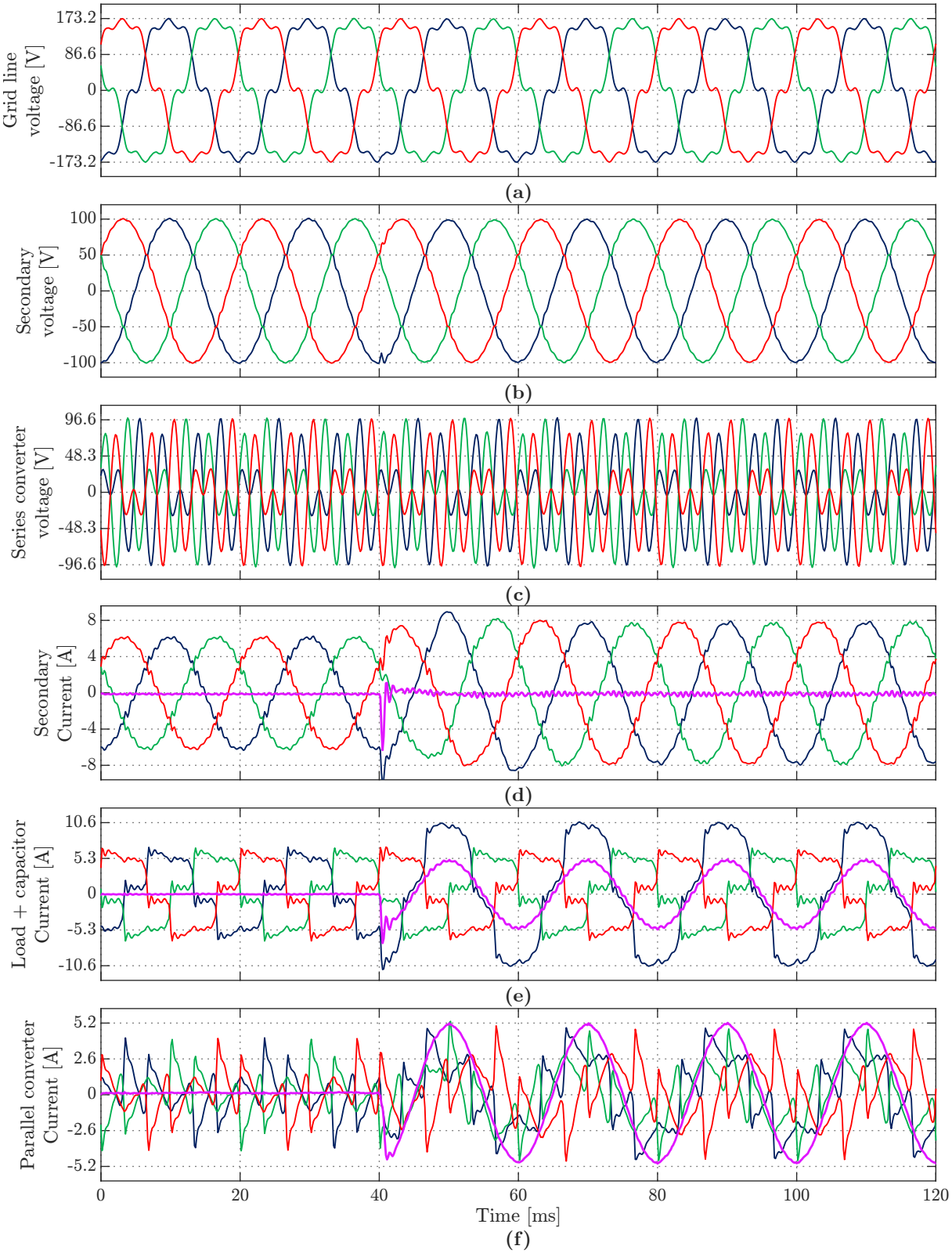


Fig. 5.21. Experimental results (Microcontroller) - 4-wire grid - Dynamic response of the HDT under a neutral-connected load step with a distorted grid. **(a)** Grid line-to-line voltage. **(b)** Secondary-side voltage. **(c)** Series converter voltage. **(d)** Secondary-side current. **(e)** Load current. **(f)** Parallel converter current.

5.5 Conclusion

This chapter presented the discrete-time control of the HDT based on a series converter connected to the MV side and a parallel converter connected to the LV side. Both converters are controlled utilizing discrete-time LQR, which includes resonant terms to compensate for the load current and grid voltage harmonics. As LQR is a state-feedback controller, the stability problems associated with the resonances of LC and LCL filters are solved, as shown in the simulation and experimental results.

The results presented in this work confirm that the proposed HDT configuration at slight CAPF is suitable for improving PQ issues, such as voltage sags, swells, power factor, current, and voltage distortion, including the operation under reverse power flow. Depending on their nature, the proposed HDT controller compensates for the disturbances in between half and a cycle. While operating under distorted conditions, the proposed configuration reduces the current and voltage THD on the LFT terminals, which diminishes its losses and extends its lifetime, consequently. Additionally, the successful operation of the HDT in a 4-wire grid was shown, in which the 4th leg of the parallel power converter is utilized to mitigate the common-mode current of the load, therefore improving the quality of the currents flowing on the main LFT.

Chapter 6

PROOF OF CONCEPT: FLUX REGULATION

Remark: This chapter is partly based on the following publication of the author:

[1] A. Carreno, M. Perez and M. Malinowski, "Flux Compensation in a Hybrid Transformer with the Series Converter Connected on the Primary-Side," *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2023.

HDTs that connect their series converters to the secondary can regulate the load voltage. The primary side is directly connected to the grid, such as a conventional LFT. Under voltage disturbances, e.g., a voltage sag, the flux of the transformer is affected, and a DC flux offset is present in the magnetic core of the transformer. When the voltage sag is restored, the combined action of the DC flux offset and the rated peak-to-peak flux amplitude can take the magnetic core into the saturation zone, generating high amplitude inrush currents. These high-amplitude currents can jeopardize the safety and correct operation of the electrical grid [112].

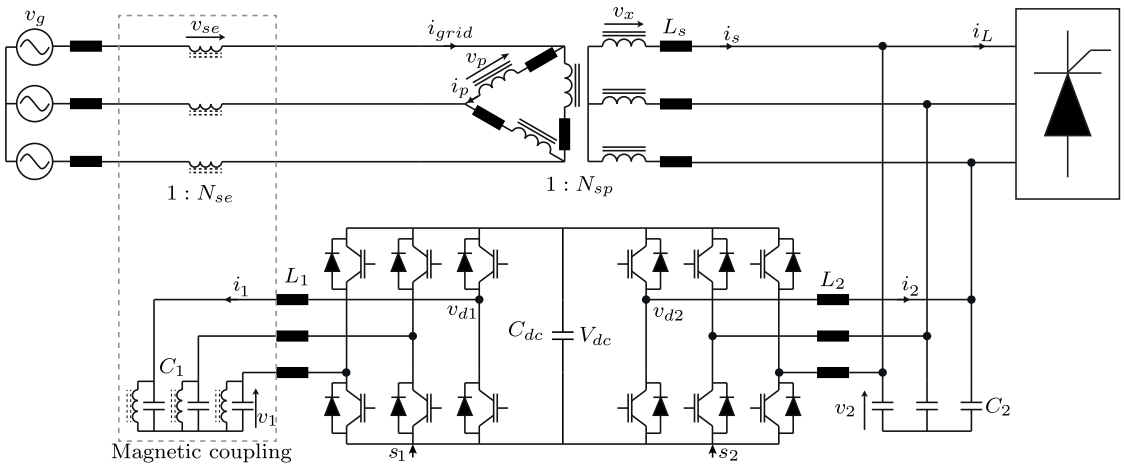


Fig. 6.1. HDT configuration with a series converter on the primary side and a parallel converter on the secondary side.

Most control strategies of series converters are based on modifying the injected voltage to avoid the saturation of the Coupling Transformers (CTs). It is possible to minimize the saturation of the CTs by reducing the injected voltage to zero [113]. Consequently, this operation will distort the transformer or load voltage until the CT is out of the saturation zone. Some alternatives are proposed to eliminate the DC magnetic flux of the CTs. For example, once a voltage sag occurs, the control system waits until the grid voltage reaches its peak to start injecting the compensation voltage [114]. Some variations of this method include injecting half of the required voltage for half a cycle and then proceeding to provide total compensation or reducing to zero the compensation during one-sixth of the period [114]. On the other hand, a solution where the CTs magnetizing branch is considered in the control loop allows adopting a linked flux feedback control, which effectively reduces the DC offset and reduces the inrush current generation [115]. These methods are presented as solutions to regulate sensitive loads.

The series converter connected to the primary side can mitigate grid voltage disturbances to have a regulated voltage on the primary of the main LFT. Nonetheless, this does not guarantee that the flux of the transformer is controlled. Therefore a DC flux offset may still exist, which could generate inrush currents under certain grid conditions. Therefore, a controller that considers the flux of the main LFT is proposed for the series converter as a proof of concept. The objective of the controller is to modify the injected voltage by the series controller in order to eliminate the DC offset of the flux and provide rated flux to the main LFT. With this controller, the transformer can operate under its rated BH curve during and after the voltage disturbance is applied.

The HDT configuration used in this chapter is presented in Fig. 6.1. The neutral

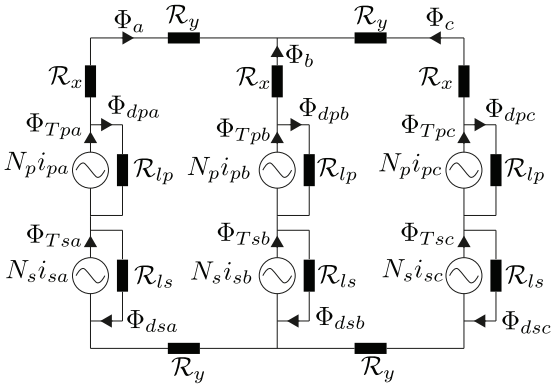


Fig. 6.2. Distribution transformer magnetic circuit.

connection of the secondary side is neglected because this chapter focusses on the series converter, which is connected to the primary side. Therefore, the common mode components of the secondary side are not transferred to the medium voltage side due to the main LFT winding configuration.

6.1 Three-legged distribution transformer magnetic model

The magnetic circuit of the HDT is presented in Fig. 6.2, and as $\Phi_a + \Phi_b + \Phi_c = 0$, the system equations can be written as follows,

$$N_p \mathbf{K_n} i_p + N_s \mathbf{K_n} i_s = \boldsymbol{\mathcal{R}}_{\mathbf{abc}} \Phi \tag{6.1.1}$$

where N_p and N_s are the primary a secondary winding turns, $\boldsymbol{\mathcal{R}}_{\mathbf{abc}}$ corresponds to the reluctance matrix of the DT, and $\mathbf{K_n}$ corresponds to the floating neutral matrix. If $\mathcal{R}_x$ and $\mathcal{R}_y$ are the limb and yoke reluctances, respectively, then $\boldsymbol{\mathcal{R}}_{\mathbf{abc}}$ is given as follows,

$$\boldsymbol{\mathcal{R}}_{\mathbf{abc}} = \begin{bmatrix} \mathcal{R}_x + 2\mathcal{R}_y & 2\mathcal{R}_y/3 & 0 \\ 0 & \mathcal{R}_x + 2\mathcal{R}_y/3 & 0 \\ 0 & 2\mathcal{R}_y/3 & \mathcal{R}_x + 2\mathcal{R}_y \end{bmatrix} \tag{6.1.2}$$

and the phase-to-neutral matrix is

$$\mathbf{K_n} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{6.1.3}$$

The total flux circulating through the primary and secondary windings are $\Phi_{Tp} = \Phi + \Phi_{dp}$ and $\Phi_{Ts} = \Phi + \Phi_{ds}$. Φ_{dp} and Φ_{ds} are the leakage fluxes. The linked fluxes are given by $\lambda_p = N_p\Phi_{Tp}$ and $\lambda_s = N_s\Phi_{Ts}$. Therefore, the voltage equations can be written in terms of the leakage inductances and the copper losses, R_p and R_s, as follow,

$$v_p = R_p i_p + (L_{lp}\mathbf{I} + \mathbf{L_{mabc}})\frac{di_p}{dt} + N_{sp}\mathbf{L_{mabc}}\frac{di_s}{dt} \tag{6.1.4}$$

$$v_s = R_s i_s + (L_{ls}\mathbf{I} + N_{sp}^2\mathbf{L_{mabc}})\frac{di_s}{dt} + N_{sp}\mathbf{L_{mabc}}\frac{di_p}{dt} \tag{6.1.5}$$

where $\mathbf{L_{mabc}} = N_p^2\boldsymbol{\mathcal{R}}_{\mathbf{abc}}^{-\mathbf{1}}\mathbf{K_n}$ is the magnetizing inductance reflected to the primary-side. Previous equations can be written in $\alpha\beta$ coordinates. In this case, the γ component are zero, due to the delta winding configurations. Also, the primary-side current can be written in terms of the grid current utilizing a transformation matrix.

$$v_p = R_p\mathbf{K_T^{-1}}i_g + (L_{lp}\mathbf{I} + \mathbf{L_m})\mathbf{K_T^{-1}}\frac{di_g}{dt} + N_{sp}\mathbf{L_m}\frac{di_s}{dt} \tag{6.1.6}$$

$$v_s = R_s i_s + (L_{ls}\mathbf{I} + N_{sp}^2\mathbf{L_m})\frac{di_s}{dt} + N_{sp}\mathbf{L_m}\mathbf{K_T^{-1}}\frac{di_g}{dt} \tag{6.1.7}$$

$\mathbf{K^T}$, defined in (2.4.8), is the rotation matrix used to transform from phase to line voltages.

$$\mathbf{K} = \frac{\sqrt{3}}{2}\begin{bmatrix}\sqrt{3} & 1\\ -1 & \sqrt{3}\end{bmatrix} \tag{6.1.8}$$

The magnetizing inductance in $\alpha\beta$ coordinates is given by $\mathbf{L_m} = N_p^2\boldsymbol{\mathcal{R}}^{-\mathbf{1}}$, and the inverse of the reluctance matrix is given as follows,

$$\boldsymbol{\mathcal{R}}^{-\mathbf{1}} = \frac{1}{|\boldsymbol{\mathcal{R}}|}\begin{bmatrix}3(\mathcal{R}_x + \mathcal{R}_y) & -\sqrt{3}\mathcal{R}_y\\ -\sqrt{3}\mathcal{R}_y & 3\mathcal{R}_x + 5\mathcal{R}_y\end{bmatrix} \tag{6.1.9}$$

where $|\boldsymbol{\mathcal{R}}| = 3\mathcal{R}_x^2 + 8\mathcal{R}_x\mathcal{R}_y + 4\mathcal{R}_y^2$.

6.2 Voltage sags effects

Faraday's Law of Induction relates the voltage on the terminals of the transformer with its magnetic flux. Assuming that the grid impedance is negligible, the flux of the transformer can be approximated to the integral of the grid voltage. Under and after grid voltage disturbances, such as voltage sags or swells, the transformer flux is modified, possibly

leading to undesirable operation.

The per unit grid voltage, assuming that it suffers a voltage sag or swell and then is taken back to its regular operation, can be modeled as follows.

$$v_g(\theta) = \cos(\theta) + K_{vp}\cos(\theta)\mu(\theta - \theta_i) - K_{vp}\cos(\theta)\mu(\theta - \theta_f) \tag{6.2.1}$$

where θ is the phase angle, and $\mu(\theta)$ is the step function. K_{vp} indicates a balanced swell and sag. θ_i and θ_f correspond to the sag/swell initial and final angle, respectively. After integrating the grid voltage, the flux can be decomposed into its AC and DC components.

$$\lambda_{AC}(\theta) = (1 + K_{vp}\mu(\theta - \theta_i) - K_{vp}\mu(\theta - \theta_f))\sin(\theta) \tag{6.2.2}$$

$$\lambda_{DC}(\theta) = K_{vp}\sin(\theta_i)\mu(\theta - \theta_i) - K_{vp}\sin(\theta_f)\mu(\theta - \theta_f) \tag{6.2.3}$$

After the sag/swell is cleared, the AC magnitude of the flux is unitary. Nonetheless, the DC component is given by the following equation.

$$\lambda_{DC}(\infty) = K_{vp}(\sin(\theta_i) - \sin(\theta_f)) \tag{6.2.4}$$

The steady-state DC components of the flux depend on the initial and final sag/swell angle difference. If both are equal, the DC flux is suppressed. Nonetheless, in most cases, the dependence between both angles is stochastic, which in most cases will generate a DC flux offset. As it is shown in Fig. 6.3, when the angle at which the voltage sag is restored differs from the angle at which the sag was applied, a flux offset will be present.

According to the magnetic characteristic of the transformer core, after the disturbance is cleared, the flux offset can shift the core into the saturation zone. The BH curve of one magnetic leg of the transformer before and after the sag is applied is shown in Fig. 6.4(a). Considering a pronounced nonlinear characteristic, a simulation is carried out, and its results are shown in Fig. 6.4(b)–(c). It can be seen that in normal operation and during the sag, the no-load currents are negligible. However, once the grid voltage is restored, high-amplitude currents are generated due to the nonlinear characteristic of the core. In this simulation case, the peak current reaches 45A.

6.3 Flux Regulation

HDT configuration of Fig. 6.1 has a voltage-controlled power converter connected on the primary side used to mitigate disturbances on the grid voltage. Therefore, the same

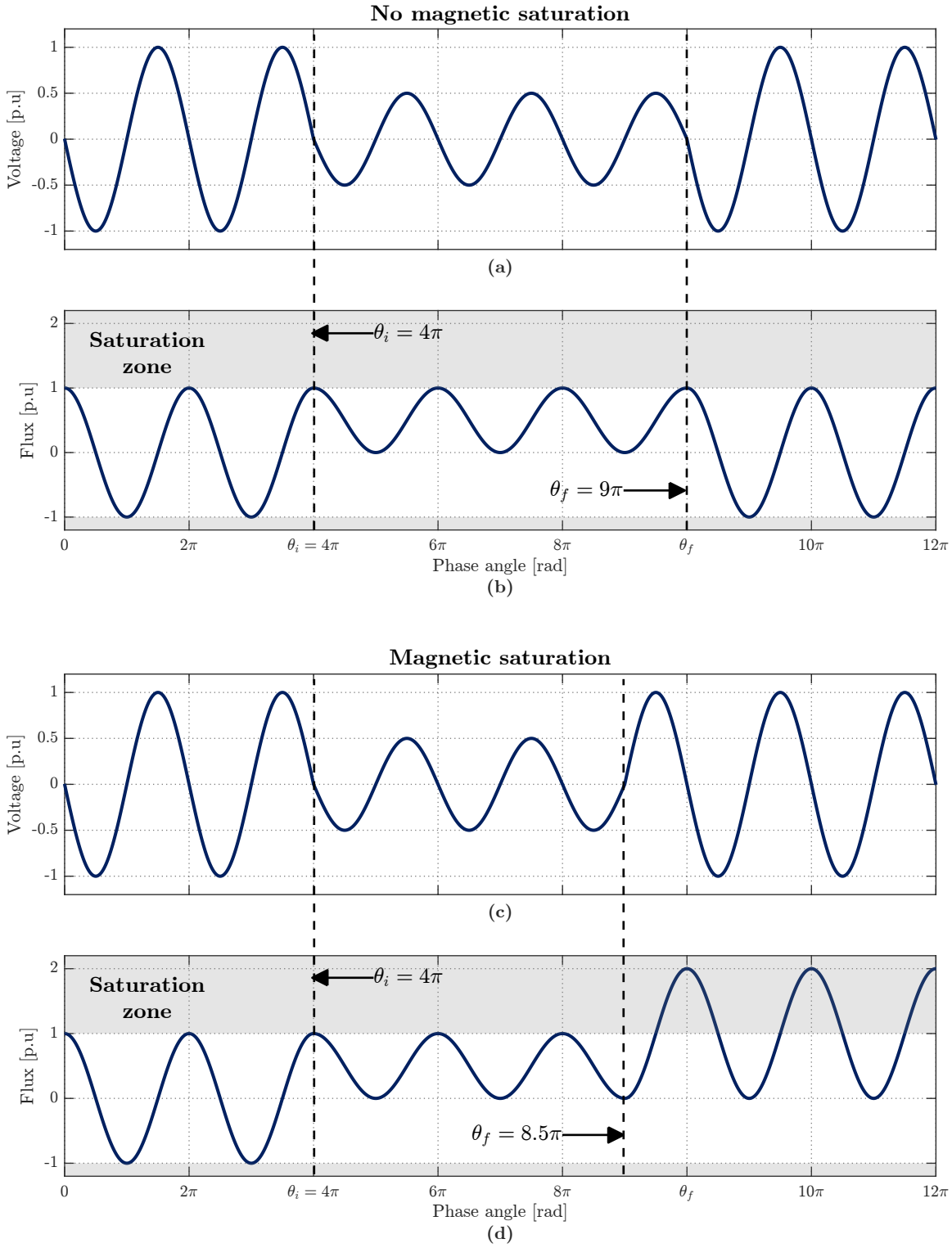


Fig. 6.3. Grid voltage and transformer flux for nonsaturated and saturated operation. **(a)** Grid voltage for nonsaturated condition. **(b)** Nonsaturated transformer flux. **(c)** Grid voltage for saturated condition. **(d)** Saturated transformer flux.

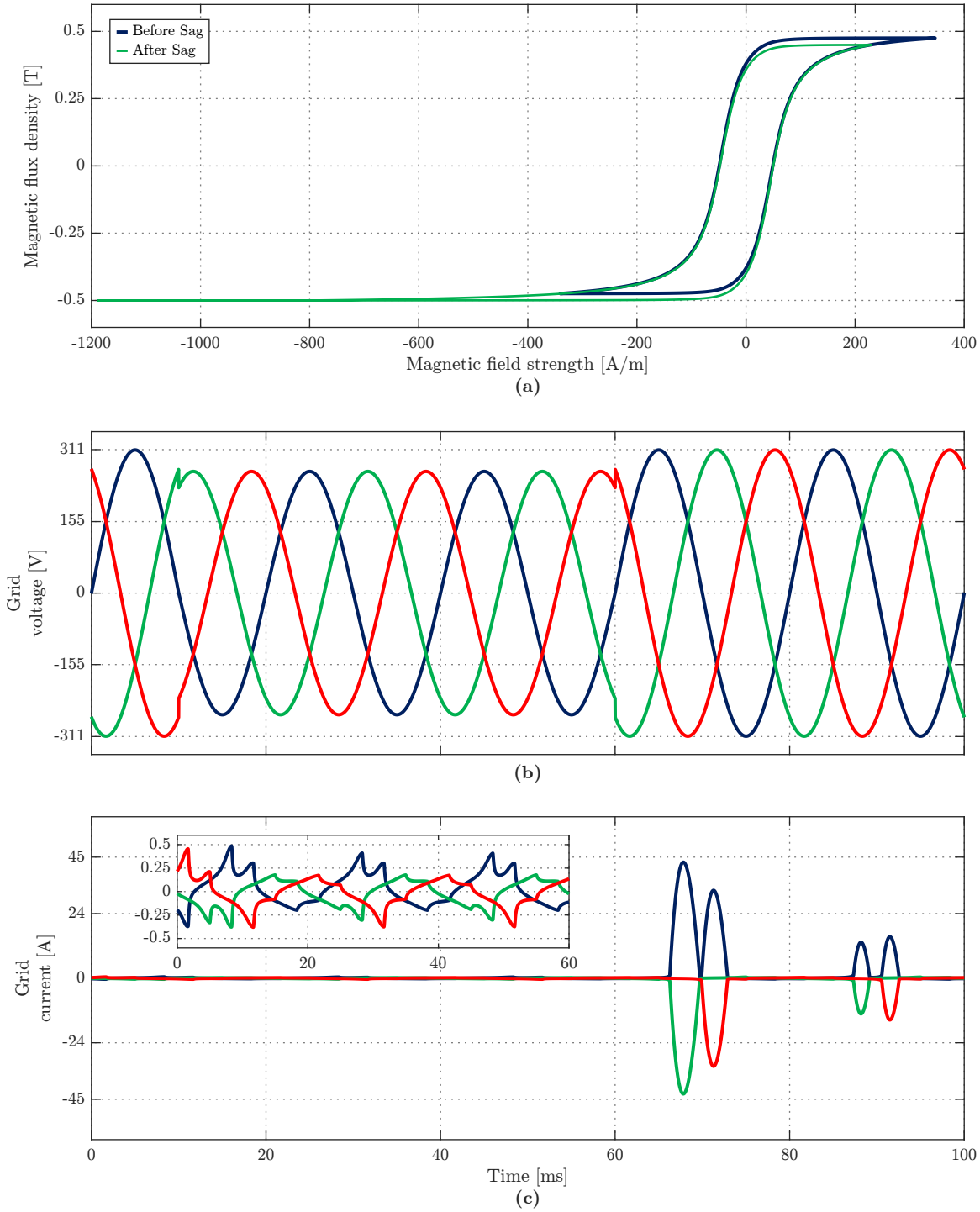


Fig. 6.4. Flux saturation - Simulation example. **(a)** Transformer BH curve during normal operation and after restoring a voltage sag. **(b)** Grid voltage. **(c)** Grid current.

converter can regulate the transformer flux during and after voltage disturbances to reduce inrush current generation.

6.3.1 Internal controllers

The internal controller presented in Fig. 6.5(a)–(b), such as the internal voltage controller of the series converter and the DC-Link voltage and internal current controller of the parallel power converter, are not in the scope of this chapter. Nonetheless, internal and DC-Link controllers developed in **Chapter 5** are employed.

6.3.2 Flux controller

A simplified flux model is utilized, neglecting the copper losses and leakage inductances. The line-to-line voltage gives the flux on each limb of the LFT on its terminal.

$$\frac{d\lambda_{\alpha\beta}}{dt} = \mathbf{K_T}^{\top} v_{g\alpha\beta} + v^{ll}_{se\alpha\beta} \tag{6.3.1}$$

where $v^{ll}_{se\alpha\beta}$ is the equivalent line-to-line series voltage injected by the converter. Considering the grid voltage as a disturbance, the LFT flux can be controlled using the capacitor voltage. Then, the transfer function between the flux and the series voltage is given as follows,

$$\frac{\lambda_{\alpha\beta}(s)}{v^{ll}_{se\alpha\beta}(s)} = \frac{1}{s} \tag{6.3.2}$$

The discrete-time equivalent system is obtained utilizing the Tustin approximation.

$$\frac{\lambda(z)}{v^{ll}_{se}(z)} = \frac{T_s}{2}\frac{z+1}{z-1} \tag{6.3.3}$$

If the system is controlled in $\alpha\beta$ coordinates, a resonant controller can be employed for the flux control. Also, the CT generates magnetizing currents, which have slow decaying components that can be considered constant. These currents affect the control performance. Therefore an integrator can be included in the flux controller to mitigate these disturbances. The discrete controller is given as follows,

$$C_\lambda(z) = \frac{az^3 + bz^2 + cz + d}{(z-1)(z^2 + 2\cos(\omega T_s)z + 1)} \tag{6.3.4}$$

The output of the flux controller is the line-to-line series voltage. Then, the capacitor reference voltage can be obtained as follows,

$$v^*_{1\alpha\beta} = \frac{1}{N_{se}}\mathbf{K_T} v^{ll*}_{se\alpha\beta} \tag{6.3.5}$$

The flux feedback signal is obtained from the flux estimator, which is explained further.

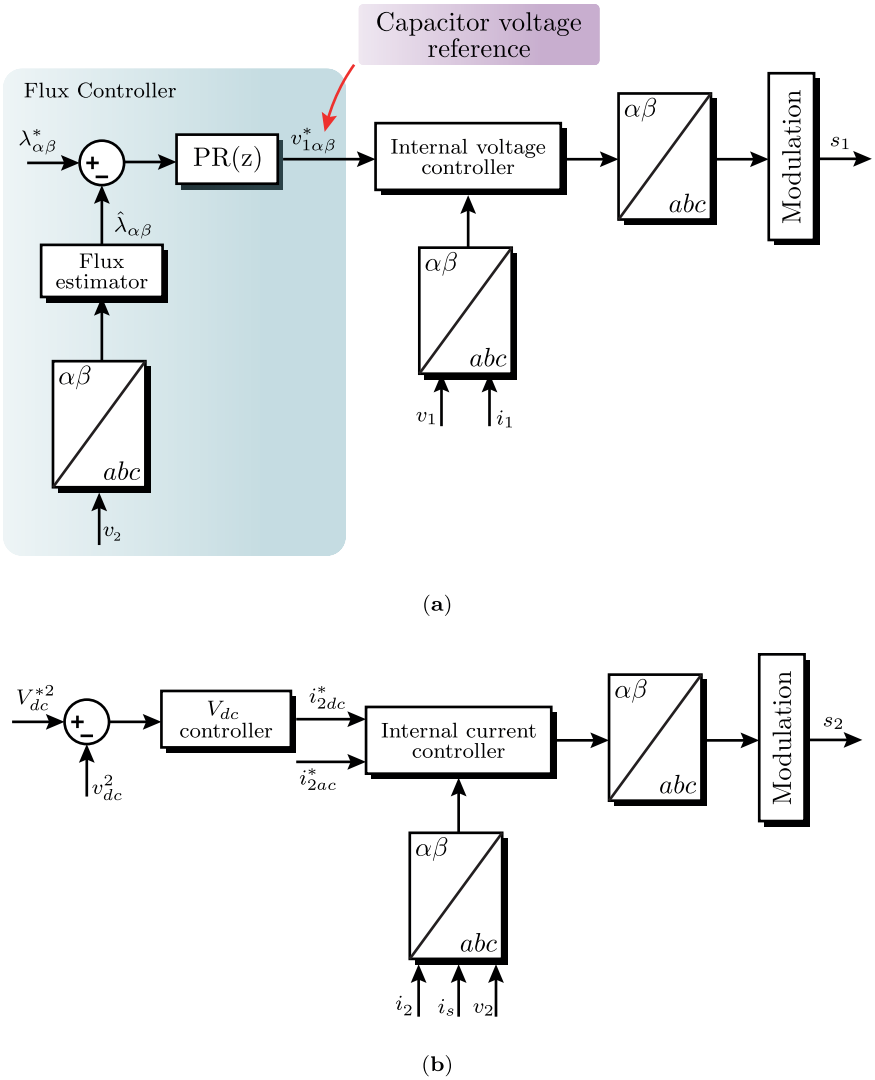


Fig. 6.5. HDT controller. **(a)** Series converter controller. **(b)** Parallel converter controller.

On the other hand, the flux reference is calculated utilizing the steady-state approximated equation, neglecting the transformer losses. The reference is obtained as follows.

$$\lambda^*_{\alpha\beta} = \frac{1}{\omega}\mathbf{K}_\mathbf{T}^\top |V_n| \begin{bmatrix} \cos(\theta_g - \pi/2) \\ \sin(\theta_g - \pi/2) \end{bmatrix} \tag{6.3.6}$$

where $|V_n|$ is the rated grid voltage and θ_g is the grid voltage phase angle, which is obtained using a Phase-Locked Loop (PLL).

When utilizing the proposed flux controller, the system regulates how the series voltage is injected, controlling its time-integral in order to mitigate the DC offset of the LFT flux and therefore mitigate the inrush current generation.

6.3.3 Flux estimator

In the previous section, it was assumed that there was a direct measurement of the LFT flux. Nonetheless, this quantity is not available, and it must be estimated.

The transformer flux can be estimated by integrating the voltage on its terminal. Nonetheless, in practical implementations, voltage measurements contain DC offset, generating a drift when integrated. One alternative is using a low-pass filter, which is designed to have a similar response at grid frequency. The low-pass filter will avoid the drift on its output due to its finite gain at DC. This is a solution used for example in Virtual Flux Oriented Control (VFOC) where the angle of the estimated flux is used for synchronization purposes.

Nonetheless, in this work, the estimated flux is given as a reference for the power converter. Therefore, if the estimated flux has a DC offset due to the low-pass filter, the output of the flux controller will generate a reference voltage that could contain a DC offset. Then, the power converter will inject a DC voltage into its output, which may saturate the CTs.

This work uses a second-order filter to estimate the LFT flux, which has a similar response at grid frequency. The frequency response is shown in Fig. 6.6, where it is compared against a pure integrator. This filter can be decomposed in terms of a high-pass and low-pass filter connected in series. The high-pass filter eliminates the impact of the DC offset of the measured voltage on the estimated flux. The Laplace transformer of the filter is given as follows.

$$H_f(s) = \frac{s}{s^2 + 2\omega_f s + \omega_f^2} \tag{6.3.7}$$

where ω_f is used to configure the bandwidth of the flux estimator. For convenience, the input of the estimator is the secondary-side voltage

6.4 Simulations Results

This section presents the simulation results of the HDT operating with the proposed flux controller. Two different scenarios are shown, which correspond to the HDT in no-load operation and supplying a nonlinear load. In both cases, the system is affected by a voltage sag. To prove the concept, an LFT with an accentuated nonlinear characteristic is employed, such as the characteristic presented in Fig. 6.4(a).

Fig. 6.7 shows the simulation results of the HDT in no-load operation mode. Fig. 6.7(a) shows the grid voltage, in which a voltage sag of 15% is applied at 40ms, which lasts for

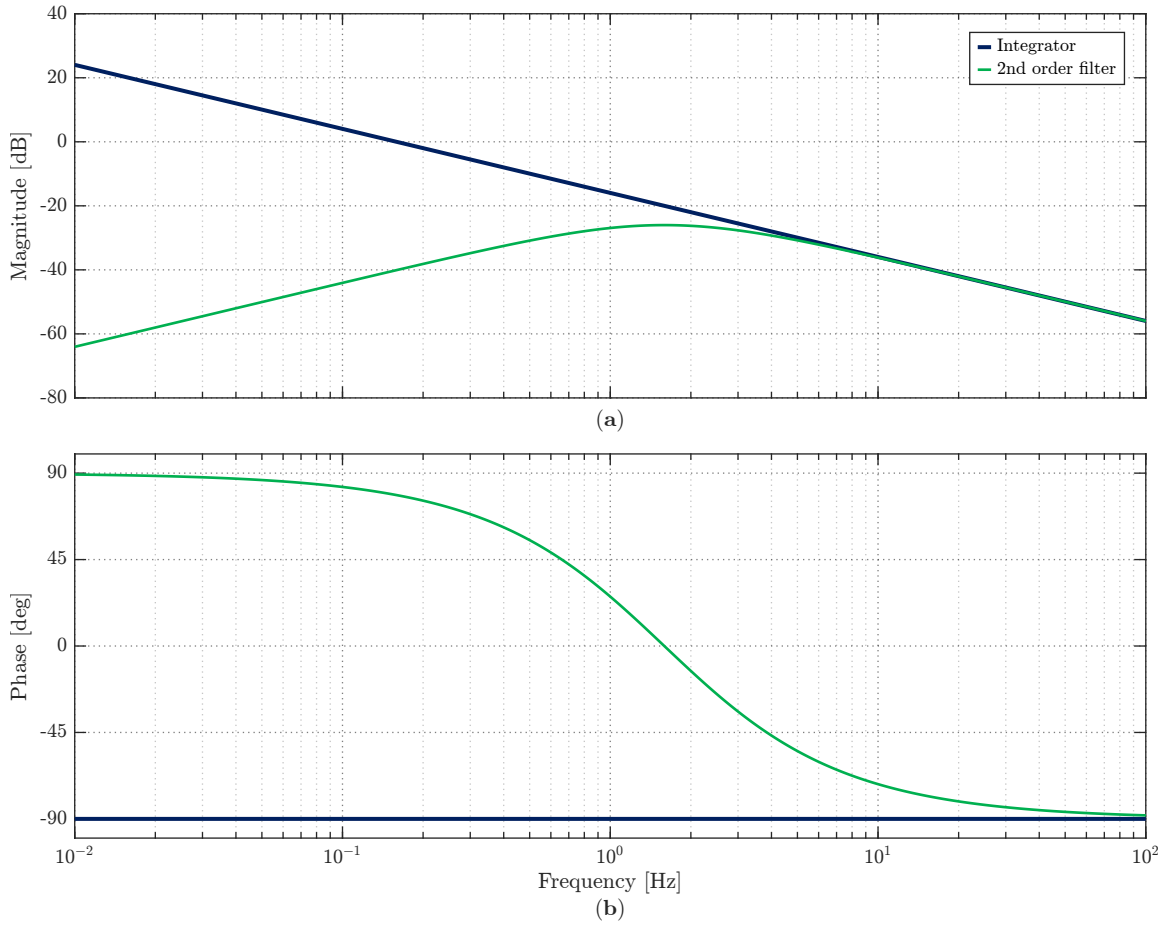


Fig. 6.6. Bode diagram of the flux estimator. **(a)** Magnitude diagram. **(b)** Phase diagram.

50ms. The flux controller generates the capacitor voltage reference in order to regulate the LFT flux. The actual voltage is presented in Fig. 6.7(b). The amplitude of the secondary-side voltage remains constant before, during, and after the voltage sag, as Fig. 6.7(c) shows. When the sag is applied, there is a visible dip in the secondary-side voltage. It can not be compensated instantly by the series converter due to its internal dynamics. Nonetheless, it mitigated in less than half of a cycle. The estimated flux is presented in Fig. 6.7(d), it can be seen that its magnitude remains constant and no DC-offset is appreciable, which is one of the objectives of the controller. A proof of the latter is presented in Fig. 6.7(e), which corresponds to the grid current. The waveforms show that, unlike results presented in Fig. 6.4, the proposed controller avoids the generation of high-amplitude currents in the LFT by canceling the DC offset of the flux, and therefore avoiding the core saturation. Nonetheless, it can be seen that after the sag is cleared, the transformer currents slightly increase, which is due to the fact that the series converter must decrease its output voltage, and this operation can not be done

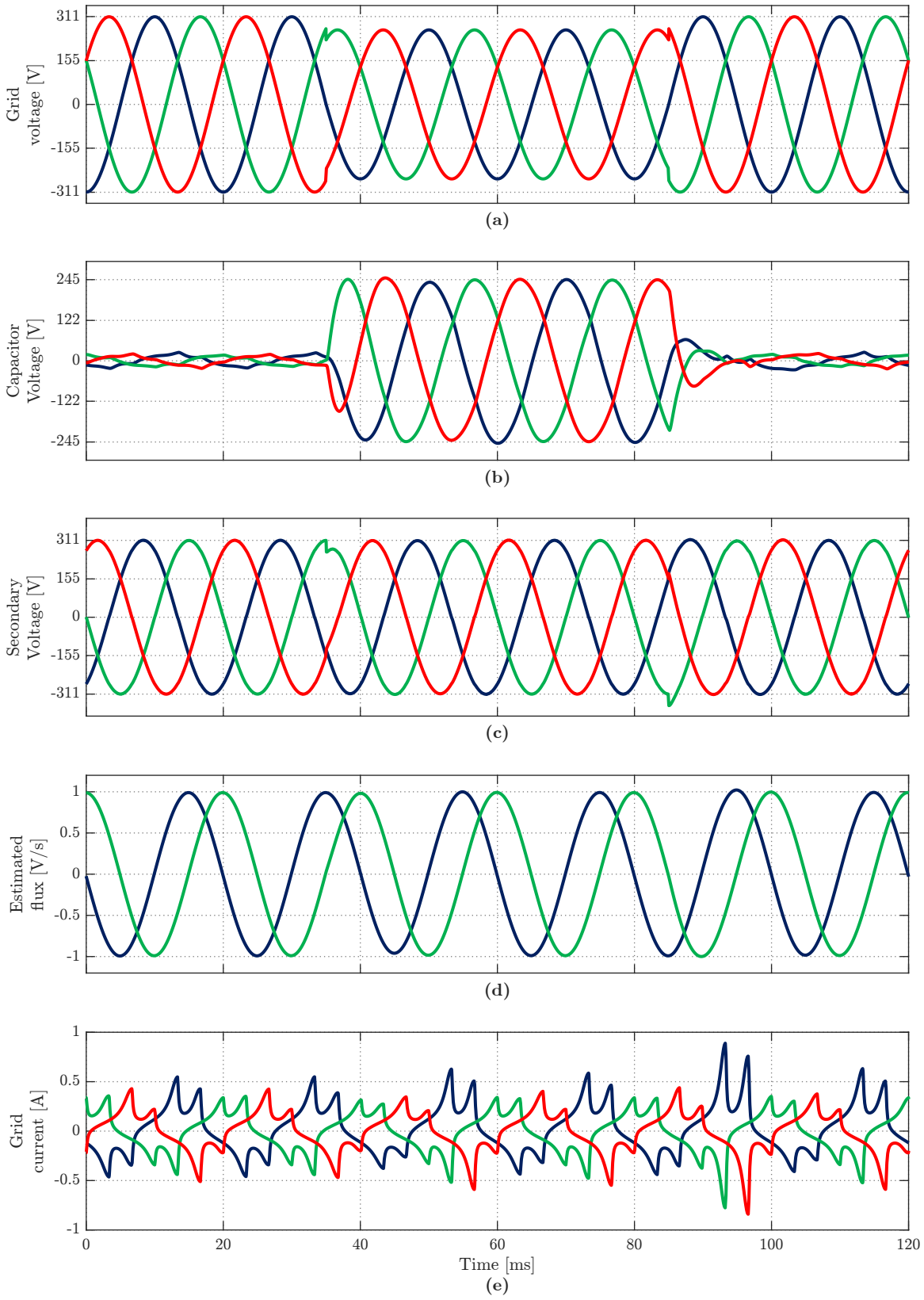


Fig. 6.7. Simulation results under a voltage sag and no-load.**(a)** Grid voltage. **(b)** Capacitor voltage. **(c)** Secondary-side voltage. **(d)** Estimated flux. **(e)** Grid current.

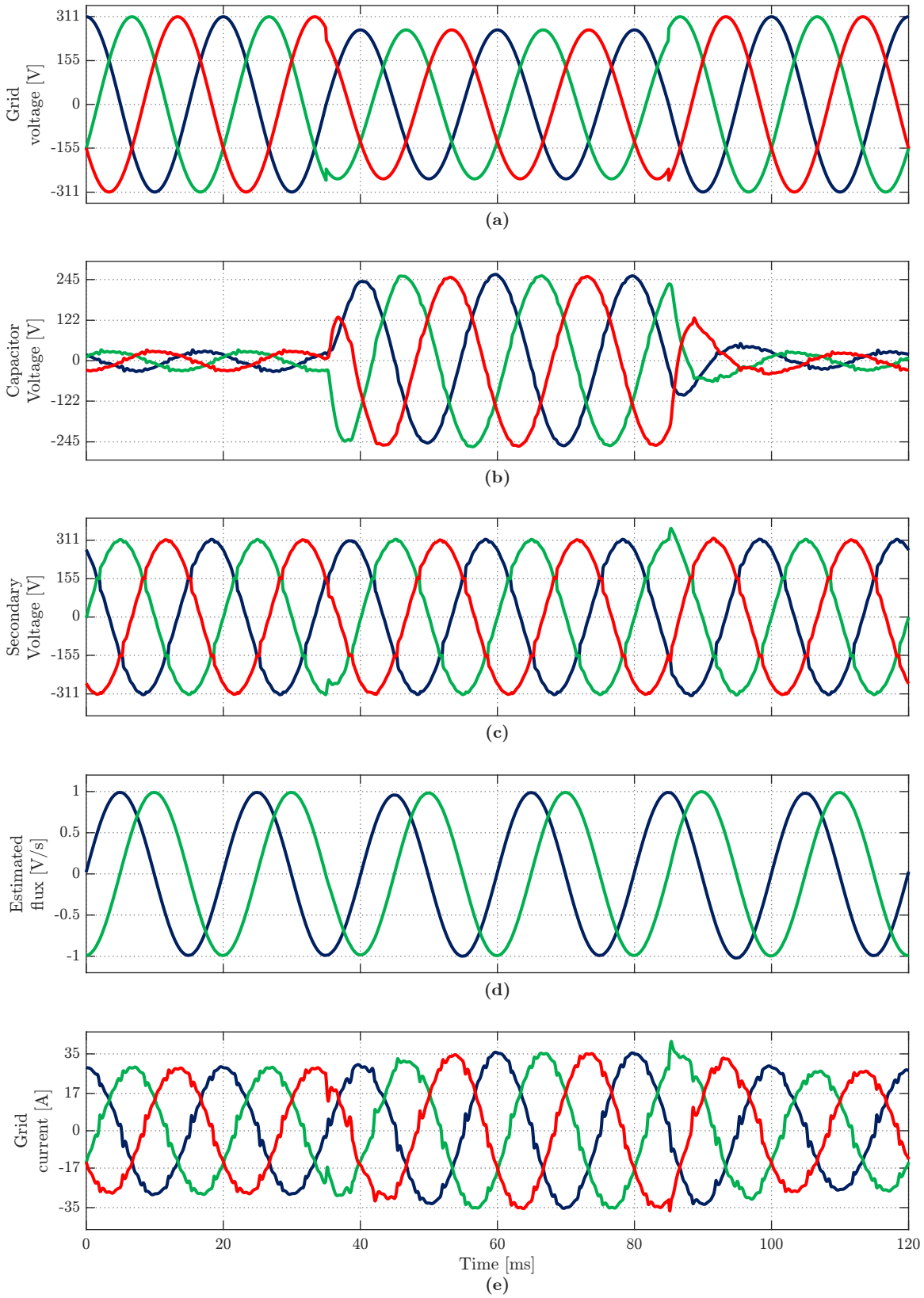


Fig. 6.8. Simulation results under a voltage sag and a nonlinear load. **(a)** Grid voltage. **(b)** Capacitor voltage. **(c)** Secondary-side voltage. **(d)** Estimated flux. **(e)** Grid current.

instantly. The peak current reaches 0.8A, approximately.

Simulation results of the HDT supplying a six-pulse bridge rectifier are presented in Fig. 6.8. As in the previous case, the system is affected by a voltage sag, which is later recovered. The parallel converter of the HDT supports the operation of the series converter by regulating the DC-Link voltage while providing power quality compensation. It can be seen in Fig. 6.8(e) that the parallel converter effectively improved the power quality by supplying the load harmonics. Nonetheless, some distortion is still appreciable in the grid current, corresponding to the harmonics currents generated by the nonlinear core of the LFT. The HDT under simulation does not eliminate these current components because it would require injecting nonlinear currents into the secondary winding. Additionally, it can be seen that during the voltage compensation, the grid current increases. This phenomenon is due to the CAPF, treated in **Chapter 4** [96].

6.5 Conclusions

The HDT used in this chapter and the proposed flux controller can effectively regulate the LFT transformer flux under voltage disturbances, eliminating the DC flux offset. Therefore, the LFT operates around its designed BH curved during and after these disturbances are applied, avoiding producing high-amplitude currents. The proposed controller was tested with an HDT operating in no-load conditions and supplying a nonlinear load. In both cases, the correct operation of the system was shown. Comparing both simulation cases and after the voltage sag is cleared, it can be seen that for the HDT with flux control, there is a reduction from 45 to 0.8A compared to a conventional LFT.

The main drawback of the flux controller comes from the flux estimation. In this work, the flux estimator is effectively working in an open loop, and therefore problems associated with the measurements offset may still exist. The next stage of the research will consider closed-loop flux estimators, in a similar manner as those utilized in induction machines.

Chapter 7

CONCLUSIONS

After a systematic review of the available HDT configurations in terms of their power converter topologies, compensation capabilities, operating regions, and applications, an HDT with a series converter on the MV side and a parallel converter on the LV side has been proposed. In comparison with other HDTs found in the literature, connecting the parallel converter to the LV winding allows for improving the current quality that flows into the main transformer of the HDT. On the other side, connecting the series converter to the MV side allows for improving the voltage quality on the windings of the transformer.

The first part of the work relied on the modeling of the HDT and its control under balanced conditions. Due to the HDT being employed in distribution grids, with high uncertainty on the grid side and load conditions, a robust control algorithm was employed. The analytical results showed that the internal stability of the HDT is maintained once both power converters are interconnected through the main transformer of the HDT. Moreover, the experimental results show a stable operation when considering the DC interconnection, and the external control loops of each converter. Therefore, the use LQR for designing the control system of the HDT is justified.

The results under balanced conditions showed that, although the HDT can regulate the load voltage and secondary current, there is an increment in the latter. Therefore, the next step of the research consisted of the study of the CAPF. The CAPF and its impact on efficiency were modeled and verified experimentally. In the conditions under study, it was

shown that the CAPF is inevitable without affecting the phase of the load voltage. The disadvantages of the CAPF are a worse utilization of the power converters and a reduction of the overall conversion efficiency. Two methods to reduce the CAPF were tested. In the first one, the series converter utilizes reactive power to provide voltage regulation. Nonetheless, high actuation voltages are required when operating at high power factors. The second method consists of utilizing a DC power source to supply the required energy during grid voltage disturbances, thus eliminating the CAPF. Therefore, the proposed HDT configuration can benefit when utilized in hybrid DC and AC microgrids.

Having analyzed the HDT under different operating conditions, a robust control algorithm was developed considering a more demanding scenario, in which the grid and load can be distorted and unbalanced. A discrete-time state-feedback control algorithm was employed for both power converters considering multi-resonant oscillators tuned at the characteristic harmonics of the power system. Estimating the grid and the capacitor voltage of the series converter, the proposed HDT can compensate for grid voltage disturbances and nonlinear load current in less than one cycle. The current and voltage THD on the terminals of the main transformer are improved. The control and experimental results of the HDT supplying a 4-wire low-voltage grid were also presented, proving its correct operation. The system stops common-mode currents from flowing through the secondary-side winding of the main transformer. Additionally, the simulation results and stability analysis showed a correct and stable operation of the HDT connected to a weak grid while processing reverse power flow.

In the last chapter of the thesis, a control algorithm to regulate the magnetic flux of the main transformer was proposed as a proof of concept. The results showed that if the estimation of the flux is obtained, then the injected series voltage can be modified in order to reduce the flux offset of the main transformer. The simulation results using a highly nonlinear transformer showed that the control algorithm effectively improves the magnetic flux, avoiding inrush currents during and after grid voltage sags and swells. Nonetheless, the method requires a correct estimation of the flux, which is highly affected by the time-varying offset of the measurements.

The research has shown that although the operation of the proposed HDT configuration requires a circulating active power flow for its operation, the control of the HDT can improve the operating conditions of the system. The proposed HDT configuration can be recognized as an alternative to SSTs to control the power flow in smart power grids. Therefore, in the opinion of the author, the thesis **"Proposing a Hybrid Distribution Transformer configuration and control algorithm, capable of improving the grid and load power quality under varying conditions, as well as improving the operation conditions of its main low-frequency transformer".**

has been proven.

In the opinion of the author, the following items developed during the doctoral work correspond to its original achievements and contributions:

- A HDT configuration with a series/parallel converter on the MV/LV side.
- Mathematical and simulation models of the proposed HDT for the different studied operating conditions.
- A discrete-time control algorithm to improve the PQ on the main transformer, grid, and load.
- Modelling and experimental verification of the losses and CAPF model of the proposed HDT.
- Proposal and applicability of two methods to reduce the CAPF.
- Proposal of a control algorithm for the improvement of the flux of the main transformer of the HDT.
- Development of an experimental setup of the proposed HDT and experimental validation of the thesis.

7.1 Future work

There are several future research paths involving the specific HDT treated in this work. Some of them are presented as follows:

- Improve the flux estimation: The flux estimator used in this work operates in open loop. Although the impact of offset of the measurements is removed in steady state, the flux estimation transient affects the flux regulation. Therefore, new closed-loop estimation methods need to be researched, such as those employed in induction machines, for example.
- Development of a simplified model of an HDT: The proposed HDT was studied locally, i.e., the analysis was focused on how the HDT behaves under grid and load disturbances. Nonetheless, power systems are complex interconnected structures. Therefore, a simplified model for large-scale simulation and also for power flow analysis is required to study the impact of the proposed HDT on the power system.

- Integration of the HDT with microgrids: It was shown that the CAPF can be eliminated by utilizing a DC source connected to the DC-Link of the HDT. Therefore, a future research path consists of the application of the HDT in microgrids, as an interface with the medium voltage grid. Several research topics arise in this area, such as the use of energy storage systems and photovoltaic systems to mitigate the CAPF, control systems of the HDT for microgrid energy management, and island operation.

- Power converter governed grids: More and more power converters are being connected to the grid. Therefore, another research path consists of the stability analysis of the HDT connected to grids with a high number of grid-tied power converters. Other robust control techniques can be studied in this regard.

Appendix A

LINEAR QUADRATIC REGULATOR

A.1 Discrete-time case

A discrete-time linear system can be represented by the following state-space representation:

$$x[k+1] = \mathbf{A}x[k] + \mathbf{B}u[k] \tag{A.1.1a}$$

$$y[k] = \mathbf{C}x[k] + \mathbf{D}u[k] \tag{A.1.1b}$$

A state-feedback control law is obtained by applying the following input.

$$u[k] = -\mathbf{K}x[k] \tag{A.1.2}$$

The linear quadratic regulator is such that the feedback gain, $\mathbf{K}$, minimizes the following quadratic cost function.

$$J = \sum_{k=0}^{\infty} \left(x^{\top}[k]\mathbf{Q}x[k] + u^{\top}[k]\mathbf{R}u[k] \right) \tag{A.1.3}$$

where the matrices $\mathbf{Q}$ and $\mathbf{R}$ are positive definite. Then, the optimal feedback gain that minimizes the cost function is obtained as:

$$\mathbf{K} = \left(\mathbf{B}^\top \mathbf{S}\mathbf{B} + \mathbf{R}\right)^{-1} \mathbf{B}^\top \mathbf{S}\mathbf{A} \tag{A.1.4}$$

and $\mathbf{S}$ is the solution of the associated algebraic Riccati equation.

$$\mathbf{A}^\top \mathbf{S}\mathbf{A} - \mathbf{A}^\top \mathbf{S}\mathbf{B}\left(\mathbf{B}^\top \mathbf{S}\mathbf{B} + \mathbf{R}\right)^{-1} \mathbf{B}^\top \mathbf{S}\mathbf{A} + \mathbf{Q} = \mathbf{S} \tag{A.1.5}$$

The design parameters for the LQR are given by the matrices $\mathbf{Q}$ and $\mathbf{R}$, which penalize the state variables and control signal.

Then, based on the matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{Q}$ and $\mathbf{R}$, the process of using the LQR is noted as follows.

$$\mathbf{K} = \mathrm{LQR}(\mathbf{A}, \mathbf{B}, \mathbf{Q}, \mathbf{R}) \tag{A.1.6}$$

The previous also applies when designing an optimal observer. Based on the duality property, the feedback gain of the observer, L, is given as follows.

$$\mathbf{L}^\top = \mathrm{LQR}(\mathbf{A}^\top, \mathbf{C}^\top, \mathbf{Q}, \mathbf{R}) \tag{A.1.7}$$

A.2 Continuous-time case

A similar approach to the one used for the discrete-time case must be followed for the continuous-time system. It is summarized as follows.

A continuous-time linear system can be represented by the following state-space representation:

$$\dot{x}(t) = \mathbf{A}x(t) + \mathbf{B}u(t) \tag{A.2.1a}$$
$$y(t) = \mathbf{C}x(t) + \mathbf{D}u(t) \tag{A.2.1b}$$

A state-feedback control law is obtained by applying the following input.

$$u(t) = -\mathbf{K}x(t) \tag{A.2.2}$$

The linear quadratic regulator is such that the feedback gain, $\mathbf{K}$, minimizes the following quadratic cost function.

$$J = \int_{t=0}^{\infty} \left(x^{\top}(t)\mathbf{Q}x(t) + u^{\top}(t)\mathbf{R}u(t) \right) \tag{A.2.3}$$

where the matrices $\mathbf{Q}$ and $\mathbf{R}$ are positive definite. Then, the optimal feedback gain that minimizes the cost function is obtained as:

$$\mathbf{K} = \mathbf{R}^{-1}\mathbf{B}^{\top}\mathbf{S} \tag{A.2.4}$$

and $\mathbf{S}$ is the solution of the associated algebraic Riccati equation.

$$\mathbf{A}^{\top}\mathbf{S} - \mathbf{S}\mathbf{A}^{\top} - \mathbf{S}\mathbf{B}\mathbf{R}^{-1}\mathbf{B}\mathbf{S} + \mathbf{Q} = 0 \tag{A.2.5}$$

The design parameters for the LQR are given by the matrices $\mathbf{Q}$ and $\mathbf{R}$, which penalize the state variables and control signal.

Then, based on the matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{Q}$ and $\mathbf{R}$, the process of using the LQR is noted as follows.

$$\mathbf{K} = \mathrm{LQR}(\mathbf{A}, \mathbf{B}, \mathbf{Q}, \mathbf{R}) \tag{A.2.6}$$

The previous also applies when designing an optimal observer. Based on the duality property, the feedback gain of the observer, L, is given as follows.

$$\mathbf{L}^{\top} = \mathrm{LQR}(\mathbf{A}^{\top}, \mathbf{C}^{\top}, \mathbf{Q}, \mathbf{R}) \tag{A.2.7}$$

Appendix B

EXPERIMENTAL SETUP

In this appendix, the experimental setup diagrams employed in each chapter are presented.

Regarding the power converters, both correspond to four-leg two-level power converters based on the Infineon FF23MR12W1M1P_B11 SiC MOSFET semiconductors. Both power converters operate at a switching frequency of 31.25 kHz, with double update PWM using a min-max modulation scheme. The 4th leg of the power converter is only utilized in **Chapter 5**, during the experimental verification of the neutral current controller.

Each power converter has direct measurements of the DC-Link voltage, and power converter output current. The remaining measurements are done in a central measurement board, which then sends the respective data to each power converter via optic fiber. All measurements are obtained using sigma-delta converters. Different measurements are used for each chapter, wich are detailed in Fig. B.1, Fig. B.2, Fig. B.3, Fig. B.4, and Fig. B.5.

All data are obtained using Tektronix MDO34 and MSO58B oscilloscopes, which are then postprocessed using MATLAB for presentation purposes. Due to channel limitation, additional results are obtained directly from the microcontrollers of each power converter and measurement board, which consequently are obtained at a lower equivalent sampling rate.

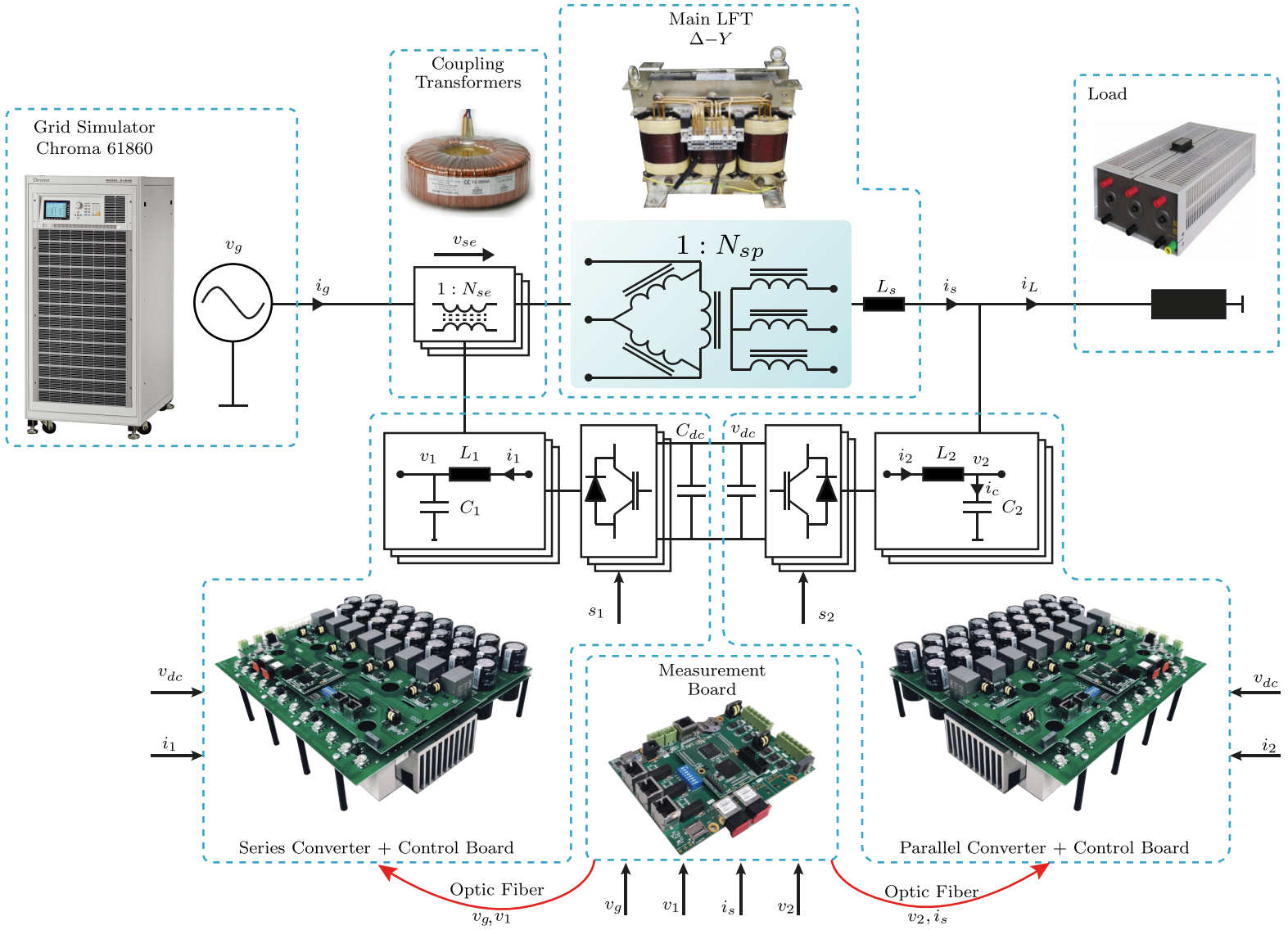


Fig. B.1. Setup diagram employed in **Chapter 3** - HDT under balanced conditions.

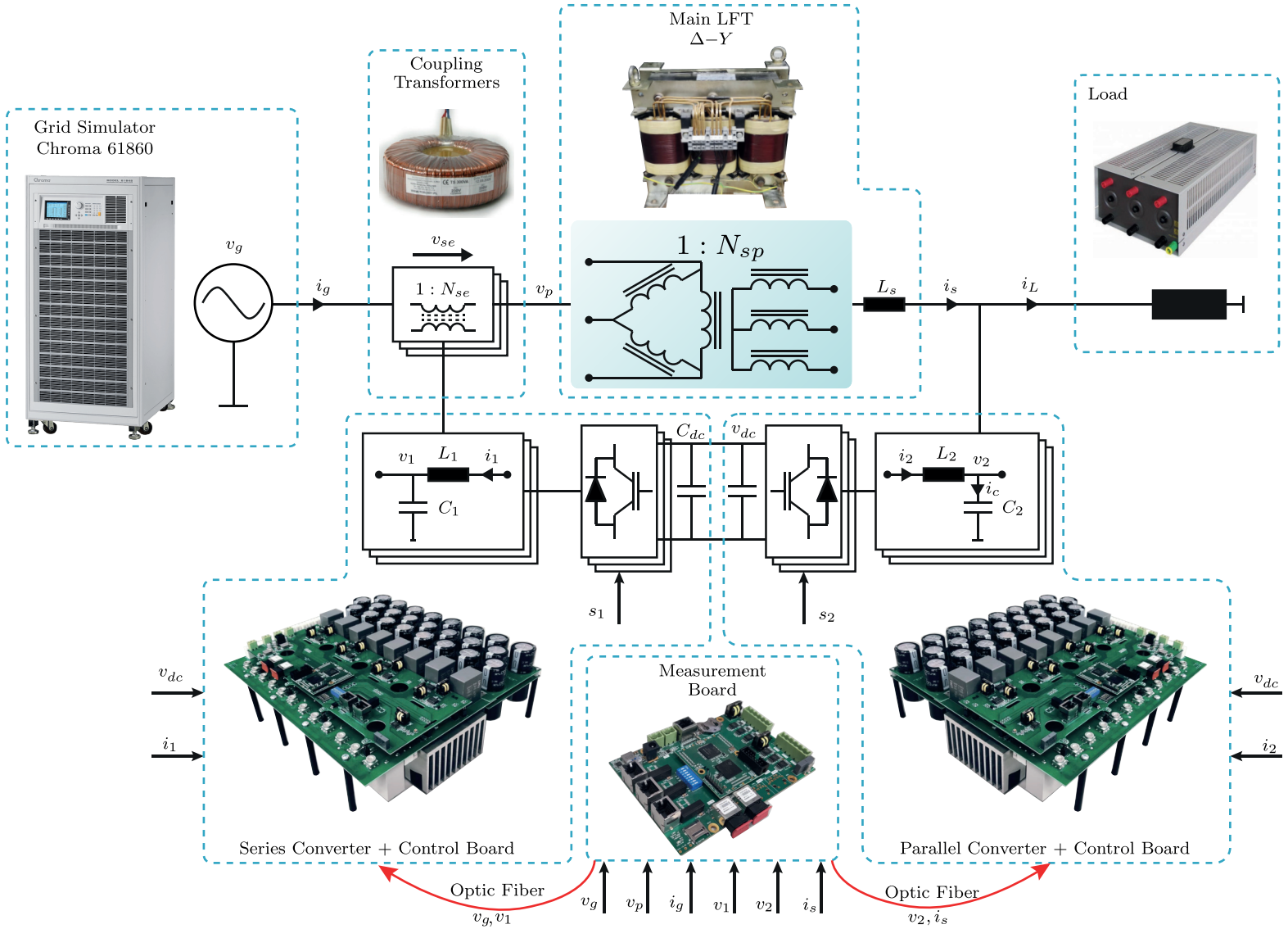


Fig. B.2. Setup diagram employed in **Chapter 4** - Efficiency experiment.

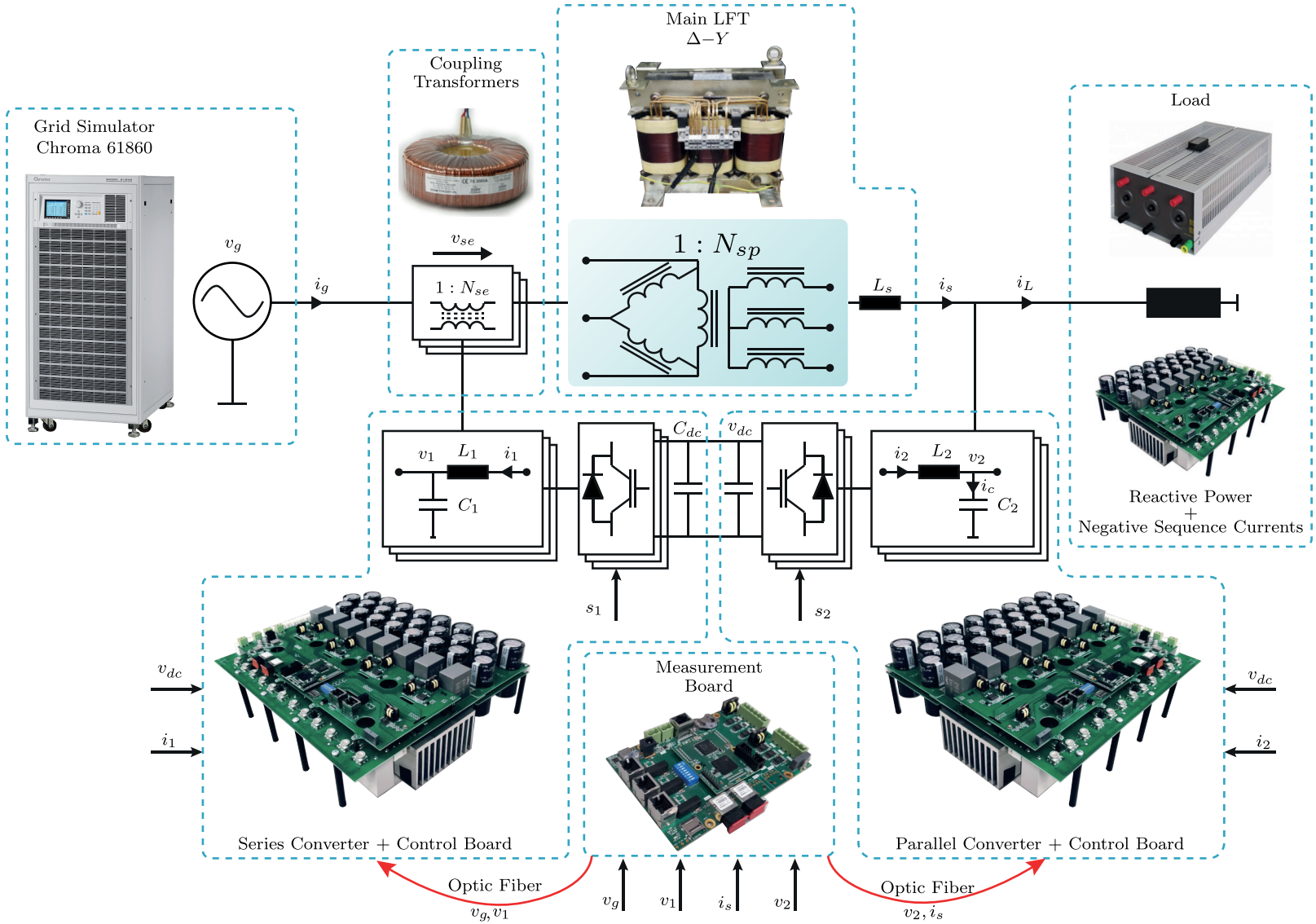


Fig. B.3. Setup diagram employed in **Chapter 4** - CAPF under unbalanced conditions and CAPF mitigation method with reactive power injection.

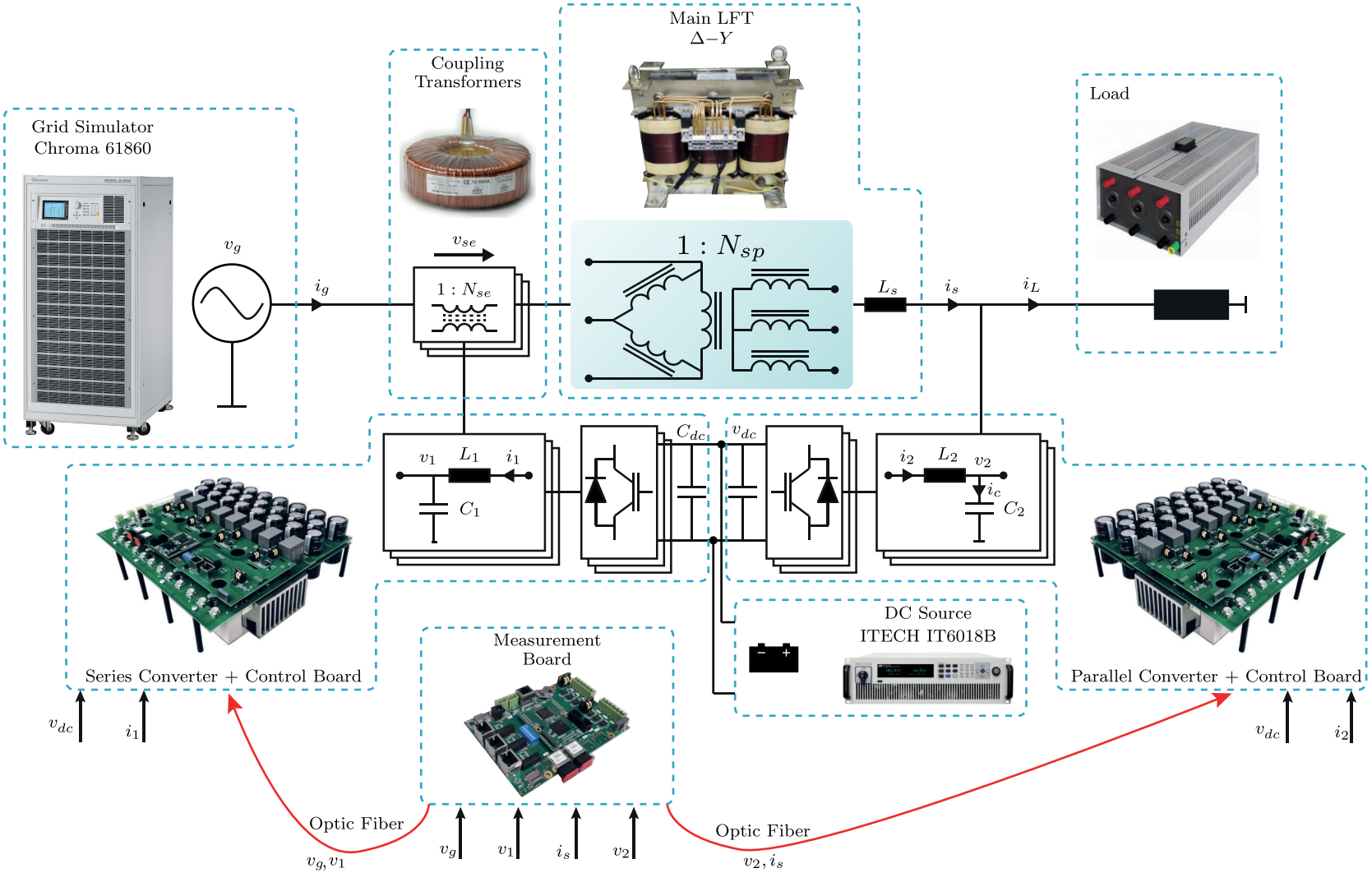


Fig. B.4. Setup diagram employed in **Chapter 4** - CAPF mitigation method with the use of a DC grid connected to the DC-Link.

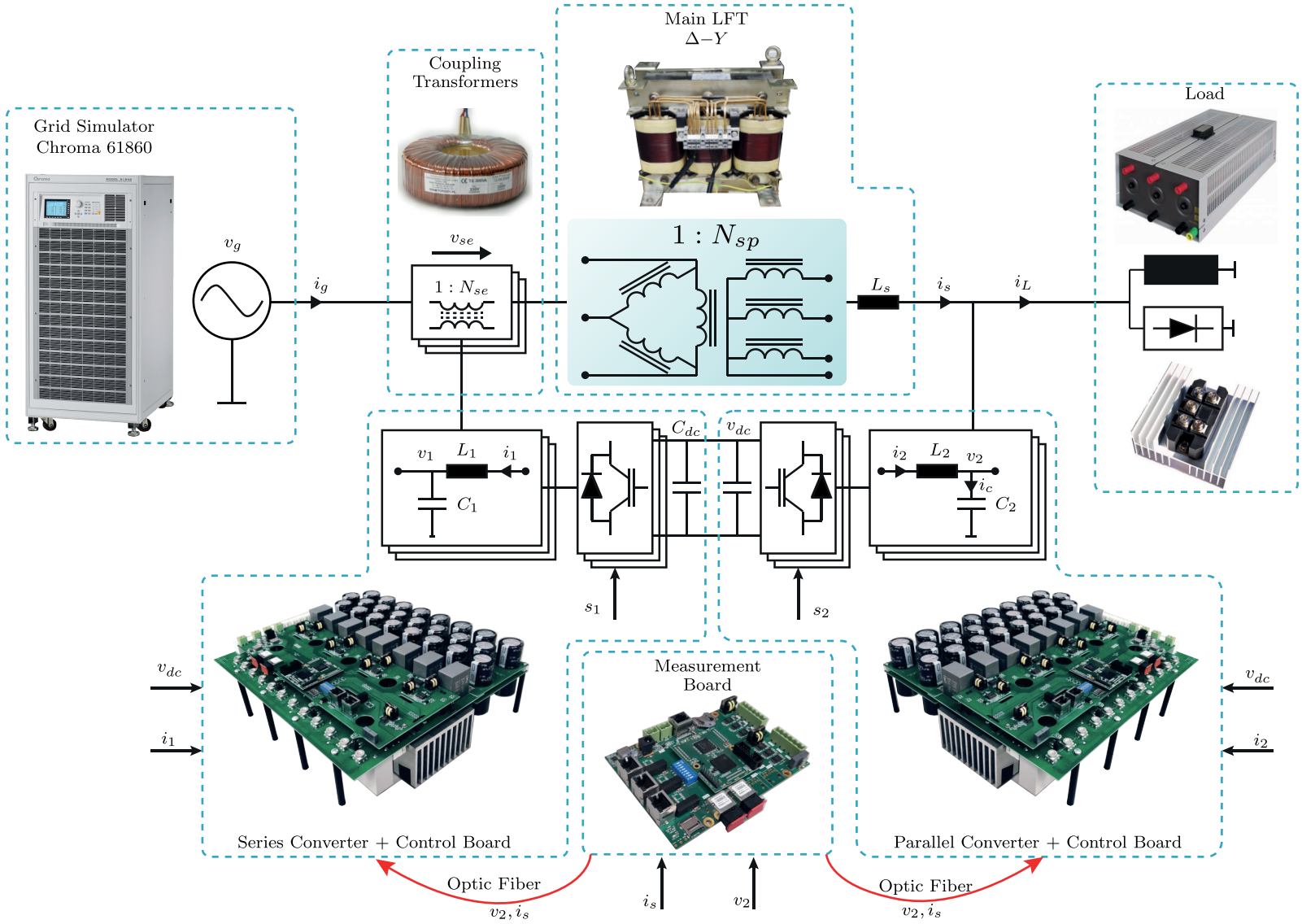


Fig. B.5. Setup diagram employed in **Chapter 5** - HDT connected to a polluted grid.

Appendix C

MV TO LV SIMULATION

This appendix shows the extension of the results shown in **Chapter 5** with simulation results of a medium voltage to low voltage 500 kVAr HDT considering the distributed parameters of a distribution line.

As Fig. C.1 shows, the main transformer of the HDT has a Δ/Y configuration with a nominal voltage of 15 kV and 400 V in the primary and secondary sides, respectively. This transformer has a short-circuit impedance of 3%.

The series stage is designed to compensate 10% of the grid voltage. For this, three single-phase CTs are employed. Therefore, the nominal voltages of the single-phase CTs are 230 V and 8.6 kV. Similarly, these transformers have a short-circuit impedance of 3%.

The medium voltage source is connected to the HDT through a distribution line. Distributed line parameters of the Polish power system can be found in [116]. The distribution line model is shown in Fig. C.2. Without taking into consideration the

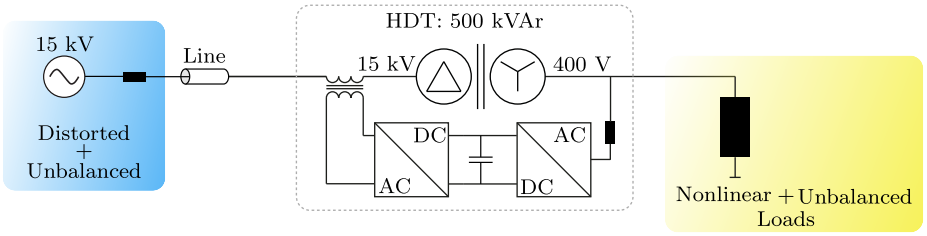


Fig. C.1. Diagram of the MV/LV HDT with distribution line.

distributed resistance, the remaining distributed parameters of the 465, 285, and 190A lines vary slightly. Therefore, for the 500kVAr system, the resistance is scaled up taking as a reference the 190A line. In this simulation, a 1 km line is employed, and its parameters are listed in Table C.1.

Regarding the load, nonlinear and unbalanced loads are employed. In this case, a three-phase rectifier with a resistive load between the phases a and b is utilized. The peak load current corresponds to 1021 A.

The simulation results are summarized as follows:

- Fig. C.3 shows the operation of the HDT under a balanced voltage sag.
- Fig. C.4 shows the operation of the HDT under a balanced voltage swell.
- Fig. C.5 shows the operation of the HDT under a distorted and unbalanced grid voltage.
- Fig. C.6 shows the operation of the HDT under a distorted and unbalanced grid voltage limiting the output current of the parallel converter to 250 A.

The results show a satisfactory operation of the HDT under an MV/LV distribution grid. The effects of the CAPF can be appreciated during the balanced voltage sag and

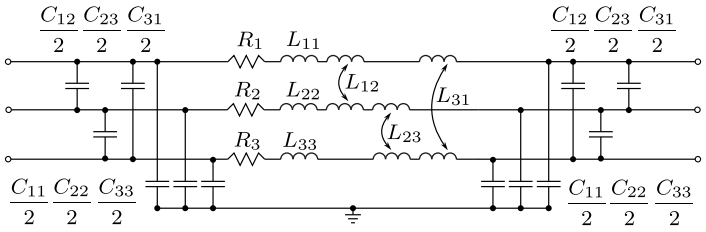


Fig. C.2. Distribution line - Distributed parameters model.

Table C.1. Adapted distribution line parameters - 500 kVAr

Parameter	Value	Unit
Resistance	$\begin{bmatrix} 7.9894 & 0 & 0 \\ 0 & 7.9894 & 0 \\ 0 & 0 & 7.9894 \end{bmatrix}$	$\frac{\Omega}{\text{km}}$
Inductance	$\begin{bmatrix} 2.4977 & 1.3408 & 1.2022 \\ 1.3408 & 2.4977 & 1.3408 \\ 1.2022 & 1.3408 & 2.4977 \end{bmatrix}$	$\frac{\text{mH}}{\text{km}}$
Capacitance	$\begin{bmatrix} 4.2261 & 2.2099 & 1.2530 \\ 2.2099 & 3.7002 & 2.2099 \\ 1.2530 & 2.2099 & 4.2261 \end{bmatrix}$	$\frac{\text{nF}}{\text{km}}$

swell. In these simulated scenarios, the HDT regulates the secondary side voltage and improves the currents through the transformer. Finally, when the output current of the parallel converter is limited to 250, it is shown that the system is still able to regulate the grid voltage disturbances, while still improving the quality of the currents of the secondary side. It must be taken into consideration that the load current is highly nonlinear and does not comply with the IEEE standards, and in more real scenarios the load currents should be filtered before being processed by the HDT.

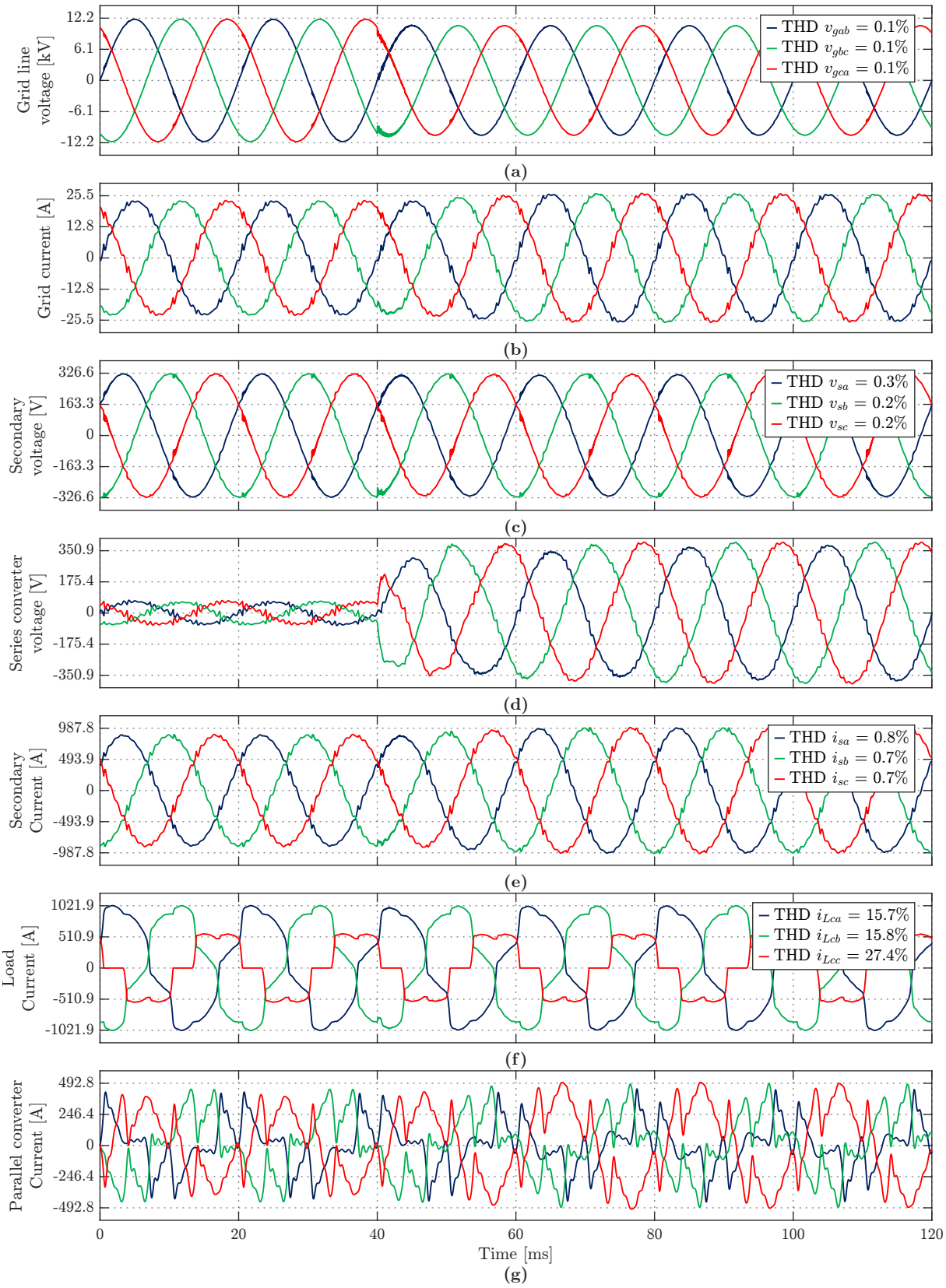


Fig. C.3. Simulation results under grid voltage sag. **(a)** Grid voltage. **(b)** Grid current. **(c)** Secondary voltage. **(d)** Series converter voltage. **(e)** Secondary current. **(f)** Load current. **(g)** Parallel converter current.

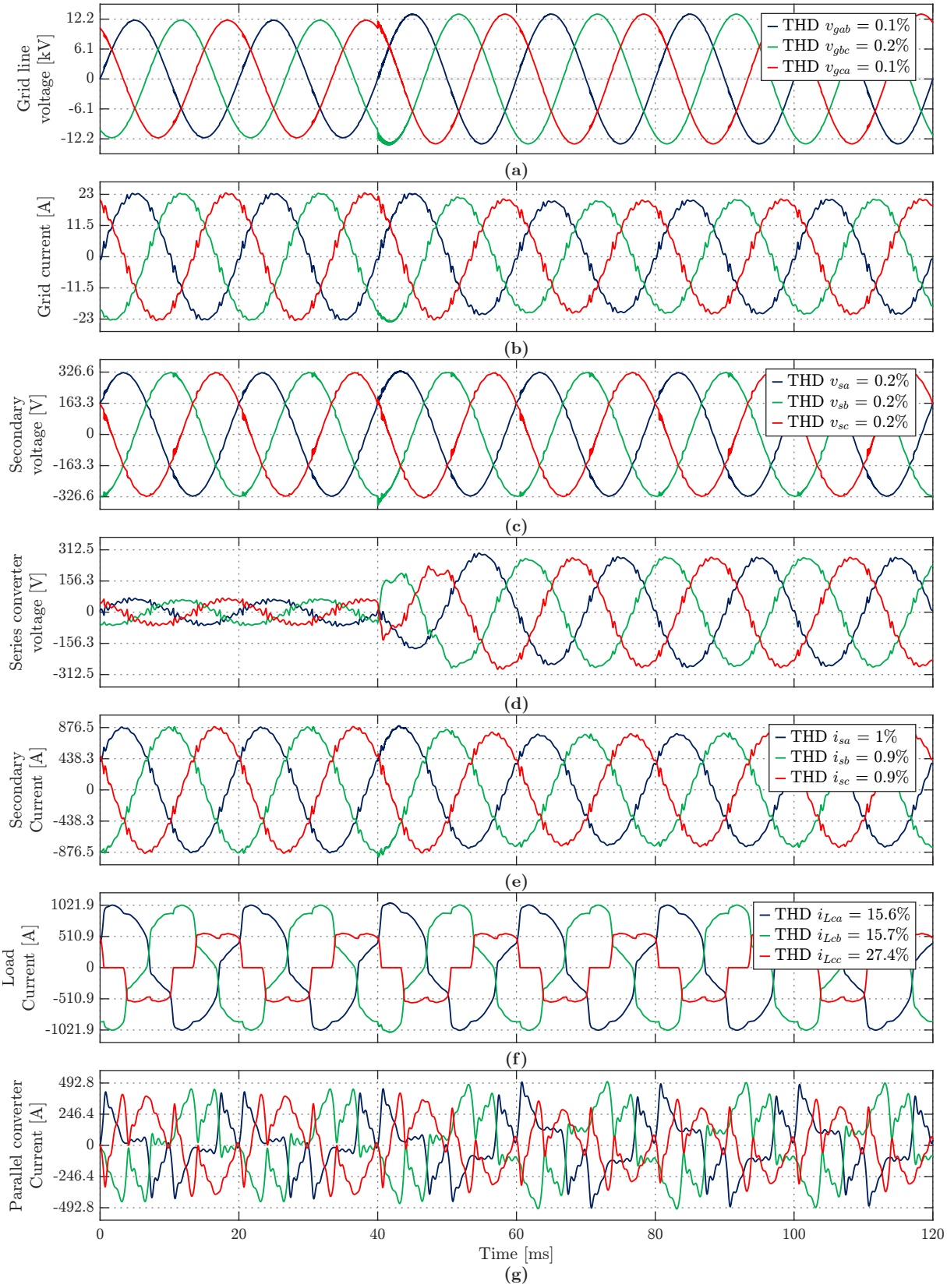


Fig. C.4. Simulation results under grid voltage swell. **(a)** Grid voltage. **(b)** Grid current. **(c)** Secondary voltage. **(d)** Series converter voltage. **(e)** Secondary current. **(f)** Load current. **(g)** Parallel converter current.

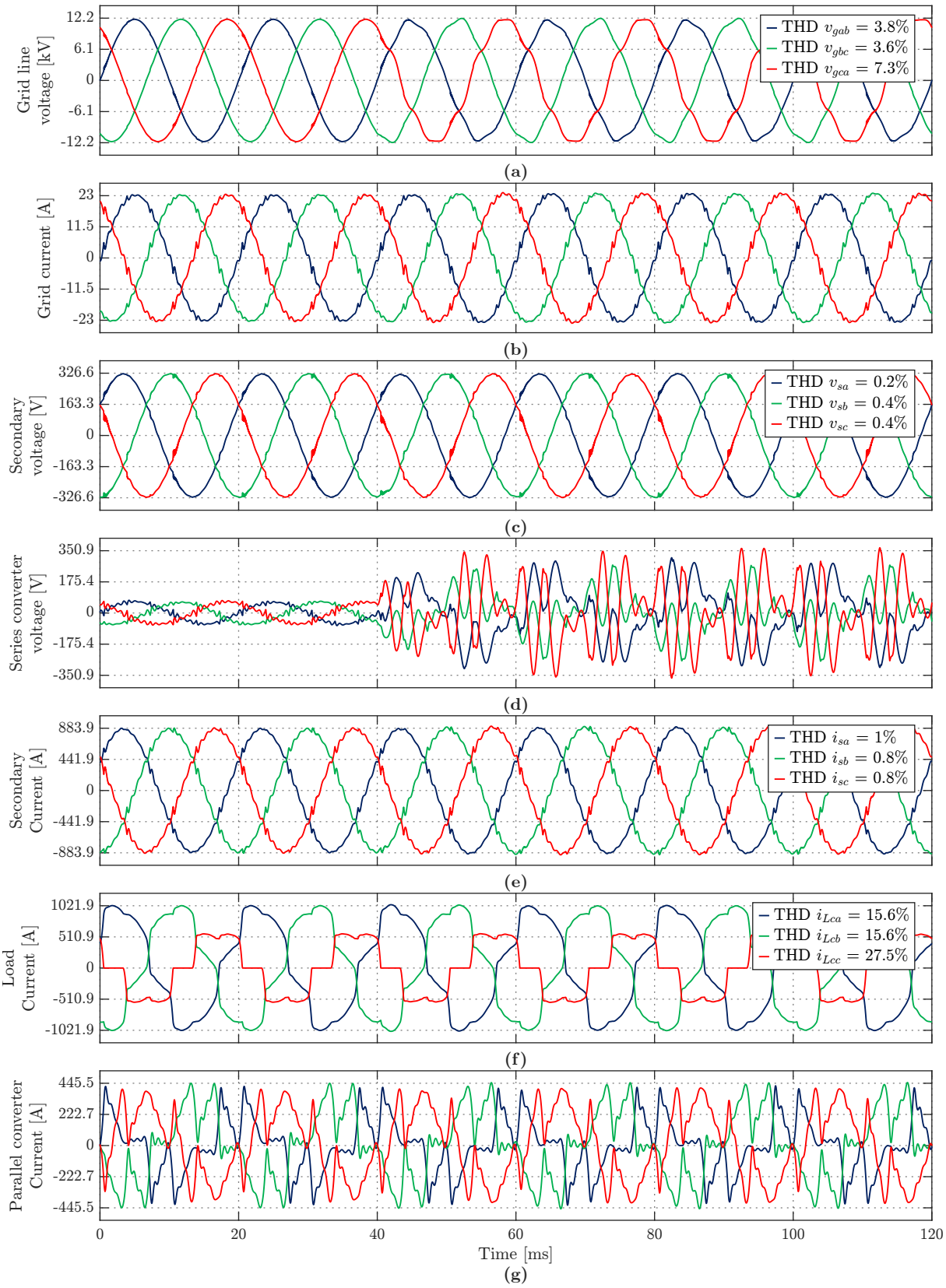


Fig. C.5. Simulation results under a distorted and unbalanced grid. **(a)** Grid voltage. **(b)** Grid current. **(c)** Secondary voltage. **(d)** Series converter voltage. **(e)** Secondary current. **(f)** Load current. **(g)** Parallel converter current.

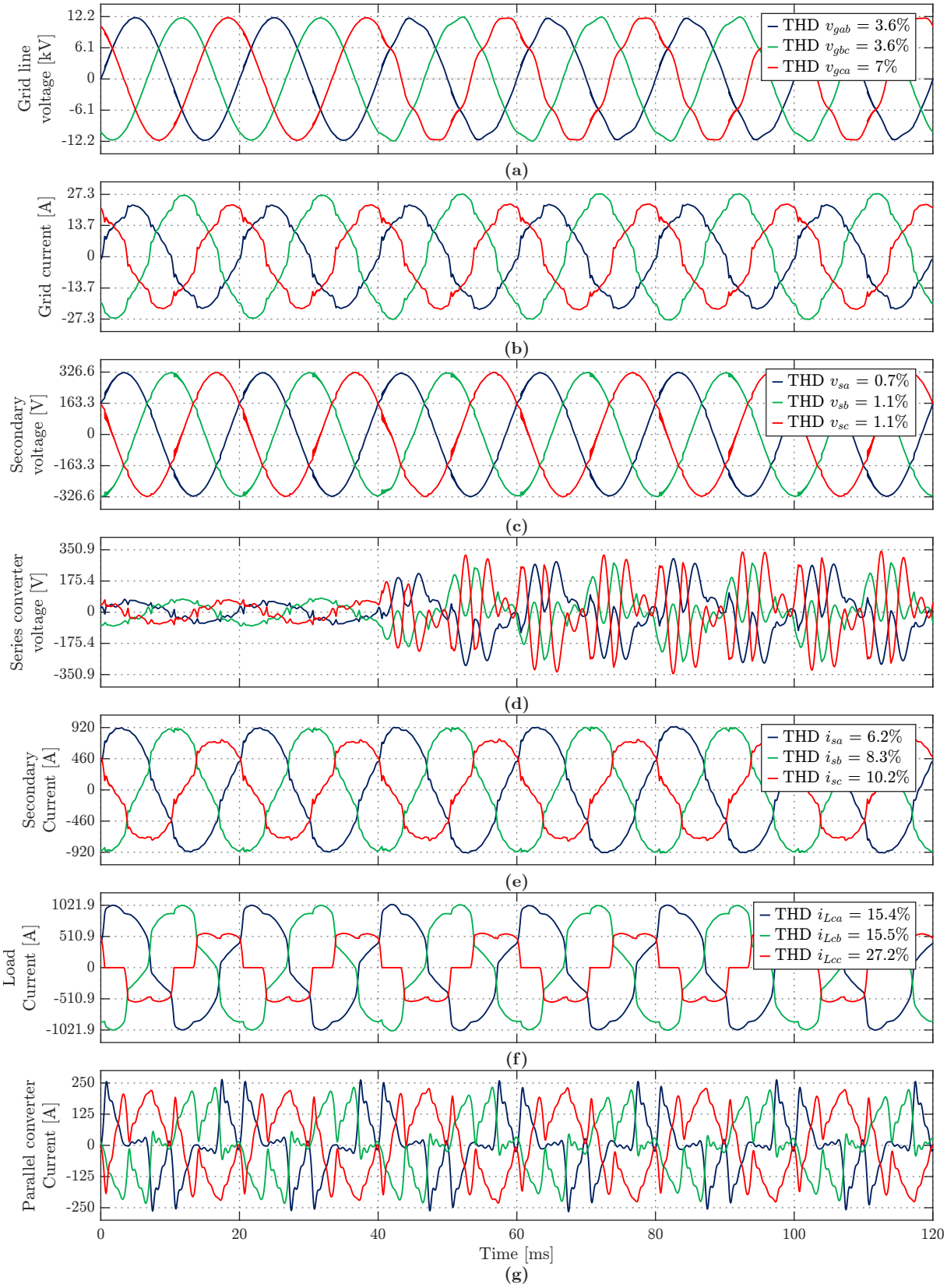


Fig. C.6. Simulation results with output current limiting. **(a)** Grid voltage. **(b)** Grid current. **(c)** Secondary voltage. **(d)** Series converter voltage. **(e)** Secondary current. **(f)** Load current. **(g)** Parallel converter current.

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